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PMOS negative bias temperature instability in an ionizing radiation environment

Geoghegan, Kevin B.

Monterey, California: Naval Postgraduate School

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MONTEREY, CALIFORNIA

DISSERTATION

PMOS NEGATIVE BIAS TEMPERATURE INSTABILITY IN AN IONIZING RADIATION ENVIRONMENT

by

Kevin B. Geoghegan

December 2013

Dissertation Supervisor: Todd R. Weatherford

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13. ABSTRACT (maximum 200 words)

As a consequence of the semiconductor industry chasing Moore's Law, device scaling and changes to the transistor material system have introduced significant emerging reliability concerns that have the potential for drastically shortening device, and hence, product lifetimes. Of these emergent reliability concerns, negative bias temperature instability (NBTI) in the p-channel metal-oxide semiconductor (PMOS) devices is widely considered the most pressing. Radiation effects and extended operating conditions commonplace in space and defense systems can exacerbate the reliability situation. This research sought to investigate the device degradation resulting from NBTI in a space-radiation environment.

In this dissertation, research and experimental results of the combined effects of NBTI and ionizing radiation on PMOS transistors manufactured in a commercially available 130 nm complementary metal-oxide semiconductor (CMOS) process are presented and discussed. For the first time, within the NBTI characterization framework, the effects of ionizing radiation on PMOS NBTI are presented.

A significant finding was that ionizing radiation had a complex effect on PMOS NBTI in which the ionizing radiation worsened NBTI at operationally relevant conditions while producing a surprisingly uncharacteristic response under higher stress conditions. Finally, a model representative of the combined effects of ionizing radiation and NBTI on the PMOS device parameters is introduced.

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PMOS NEGATIVE BIAS TEMPERATURE INSTABILITY IN AN IONIZING RADIATION ENVIRONMENT

Kevin B. Geoghegan
Civilian, United States Department of Defense
B.S., California State University, Sacramento, 1999
M.S., California State University, Sacramento, 2006

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requirements for the degree of

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December 2013

Author: Kevin B. Geoghegan

Approved by:

Todd R. Weatherford Professor of Electrical and Computer Engineering Dissertation Supervisor	Douglas J. Fouts Professor of Electrical and Computer Engineering Dissertation Co-Advisor
Sherif Michael Professor of Electrical and Computer Engineering	Monique P. Fargues Professor of Electrical and Computer Engineering
Gamani Karunasiri Professor of Physics	Jeffrey J. Siddiqui Electrical Engineer

Approved by: R. Clark Robertson
Chair, Department of Electrical and Computer Engineering

Approved by: O. Douglas Moses
Associate Provost for Academic Affairs

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LIST OF ACRONYMS AND ABBREVIATIONS

ADC	analog-to-digital converter
AFRL	Air Force Research Lab
AMS	analog and mixed signal
BOX	buried oxide
BTI	bias temperature instability
BTS	bias temperature stress
cerDIP	ceramic dual inline package
CP	charge pumping
CMOS	complementary metal-oxide semiconductor
DC	direct current
DIP	dual inline package
DMEA	Defense MicroElectronics Activity
DTS	Dewar temperature system
DUT	device under test
ELDRS	enhanced low-dose radiation sensitivity
FN	Fowler-Nordheim
HCI	hot carrier injection
HDL	Harry Diamond Labs
IC	integrated circuit
IIT	Indian Institute of Technology
JEDEC	Joint Electron Device Engineering Council
JESD	JEDEC standard
MOS	metal-oxide semiconductor
MOSFET	metal-oxide semiconductor field-effect transistor
MPM	modified process model
NET	neutral electron trap
NBTI	negative bias temperature instability
NMOS	n-channel metal oxide semiconductor
OTF	on-the-fly
PMOS	p-channel metal oxide semiconductor

PMOSFET	p-channel metal oxide semiconductor field-effect transistor
SATCOM	satellite communications
SCS	semiconductor characterization system (Keithley)
SEE	single event effects
SEGIT	Science and Engineering Gamma Irradiator Test (facility at DMEA)
SEU	single event upset
SMS	stress-measure-stress
SOI	silicon-on-insulator
TDDB	time-dependent dielectric breakdown
TID	total ionizing dose
TTF	time-to-failure

EXECUTIVE SUMMARY

For the DoD and aerospace communities, radiation effects in electronic systems and the semiconductor devices from which they are comprised have long been a concern. To complicate matters for these communities, the continued device scaling trend within the semiconductor industry has introduced significant reliability concerns that have the potential for reducing device and product lifetimes. This worrisome trend is highlighted in Figure 1. Where devices manufactured in the 1990s could be expected to last for decades, state-of-the-art devices are expected to last less than ten years.

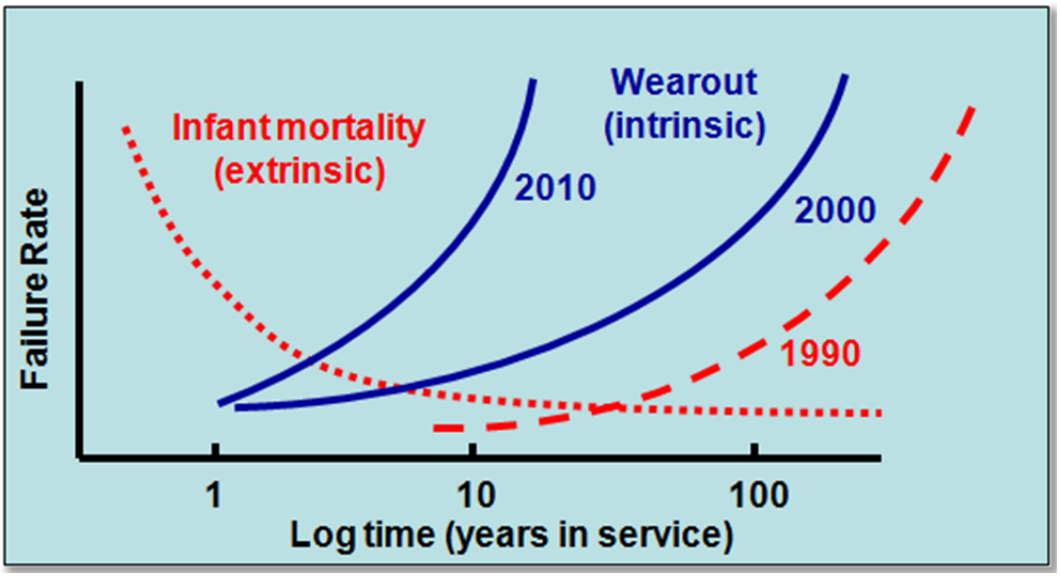

Figure 1. Generational product failure rates versus time in service, from [1].

The most pressing reliability concern today within the semiconductor industry is known as negative bias temperature instability (NBTI) in p-channel metal-oxide semiconductor field-effect transistors (PMOSFET), or PMOS NBTI. PMOS NBTI occurs when the PMOS device is subjected to a negative bias at an elevated temperature for an extended period of time. The NBTI stresses being applied to the PMOS transistor are illustrated in Figure 2. The device terminals labeled as G, S, D, and B are the gate, source, drain, and bulk terminals of the PMOS device, respectively.

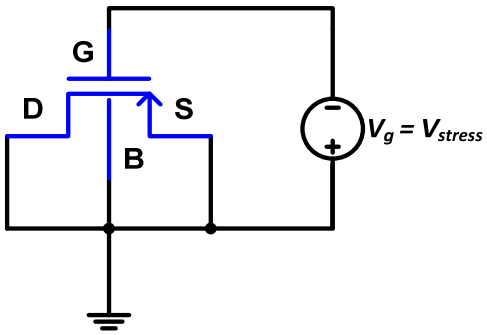

Figure 2. The PMOS transistor under NBTI stress.

The two key electrical parameters of the PMOS transistor degraded by NBTI are the device threshold voltage V_T and drive current I_{DS}. The V_T is defined as the gate voltage required to cause current to flow between the source and drain terminals resulting in I_{DS}. NBTI results in a PMOS transistor that becomes harder to turn on due to an increase in V_T and has less current capacity to drive loads due to a decrease in I_{DS}. This in turn results in slower, degraded, circuit and system performance. Radiation effects can have a similar effect on the PMOS transistor.

Research on the combined effects of PMOS NBTI and ionizing radiation on transistors fabricated in semiconductor technologies of interest to the DoD and aerospace communities is scarce. Furthermore, the physical mechanisms responsible for PMOS NBTI are a topic of hot debate within the device reliability community.

There were three main objectives of this research:

- Investigate the combined effects of ionizing radiation and NBTI stressing on the PMOS devices fabricated in a commercially available 130 nm complementary metal-oxide semiconductor (CMOS) process.
- By introducing ionizing radiation into a common PMOS NBTI device characterization framework, we gain insight into the physical mechanisms responsible for PMOS NBTI.
- Introduce a mathematical model representative of the combined effects of ionizing radiation and PMOS NBTI.

In order to achieve these objectives, experiments were performed in which the PMOS devices were subjected to negative gate bias at an elevated temperature, with and without ionizing radiation, for stress durations of up to thirty hours. During the stress duration, we periodically removed the voltage stress from the devices at regular intervals

for characterization of the device V_T and I_{DS} parameters utilizing standard MOSFET current-voltage measurement techniques. The data were later assessed for NBTI and radiation induced device parameter degradation in V_T and I_{DS}. The results were then used to make assessments as to the degree the combined effects degraded the device performance, ascribe underlying physical mechanisms to the observed effects, and introduce a model representative of the combined effects.

The results of this research were as follows:

- For PMOS devices stressed at operationally relevant bias and temperature conditions, PMOS NBTI was worsened by ionizing radiation. The extent of the additional degradation due to the combined effects was within acceptable design margins.
- The change in V_T with respect to the change in the maximum drive current I_{ON} was observed to be disproportionate in comparing the devices receiving only NBTI stress to those receiving both irradiation and NBTI stress. This surprising result indicated that the addition of radiation had a larger effect on I_{ON} than did NBTI stress alone (I_{ON}, or I_{DSAT}, is the condition for which I_{DS} is evaluated at $V_G = V_D = V_{DD}$, where V_{DD} is the maximum operating supply voltage for the process.).
- Under high stress voltage condition, the devices subjected to both ionizing radiation and NBTI stress had a very different and unexpected response compared to the devices receiving just NBTI stress. It was suspected that the radiation changed the nature of the underlying physical mechanisms responsible for NBTI. Where positive oxide charge build up in the PMOS device gate-oxide dielectric region is one mechanism responsible for the NBTI, it was surmised that this charge was being neutralized by the radiation resulting in a lessening of the change in V_T.
- From the results of this research a model was proposed that, when fully developed as the subject of future work, would account for the observed effects resulting from ionizing radiation on PMOS NBTI.

List of References

[1] L. Condra and G. Horan, "Impact of semiconductor technology on aerospace electronic system design, production, and support," in *National Software and Complex Electronic Hardware Standardization Conference*, 2005.

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I. INTRODUCTION

Reliable integrated circuits that can withstand the harsh environment of space for extended periods of time are paramount to DoD assets fielded in space. This dissertation focuses on one significant reliability issue that has the potential for jeopardizing these assets: "PMOS NBTI in an Ionizing Radiation Environment." In the sections to follow, the motivation and groundwork for the research performed in this dissertation are introduced and discussed concluding with the significant contributions of this work.

A. MOTIVATION

To an analog and mixed-signal (AMS) integrated circuit (IC) design engineer for the U.S. Department of Defense (DoD), the importance of ensuring a design will reliably function as specified in its intended operating environment over specified lifetime was understood. However, such a design engineer usually could take for granted that the reliability of the electronic devices (and thus the circuit and system as a whole) would not be a significant concern as long as the engineer followed the IC design rules for the semiconductor process in which the devices were being manufactured. That is to say device reliability was not usually the designer's foremost concern, a limiting factor, or a typical trade-off consideration such as power dissipation, speed, area, or accuracy. However, as a consequence of the semiconductor industry pursuit to keep pace with Moore's Law by aggressive device scaling and changes to the underlying material systems, device reliability has now become a major factor in the design process.

As evidenced in the curves given in Figure 1, expected product lifetimes (mean-time-to-failure) once measured in thousands of years, in semiconductor processes now measure fewer than ten; and, in some cases, less than three years in state-of-the-art semiconductor fabrication processes [1]. The reduced product lifetime may be acceptable in the portable consumer electronics market sector due to the rapid rate at which technological advances are taking place, driving consumer demand for the latest product that technology has to offer; however, this paradigm is antithetical to the requirements of DoD systems in which the product may be fielded for decades.

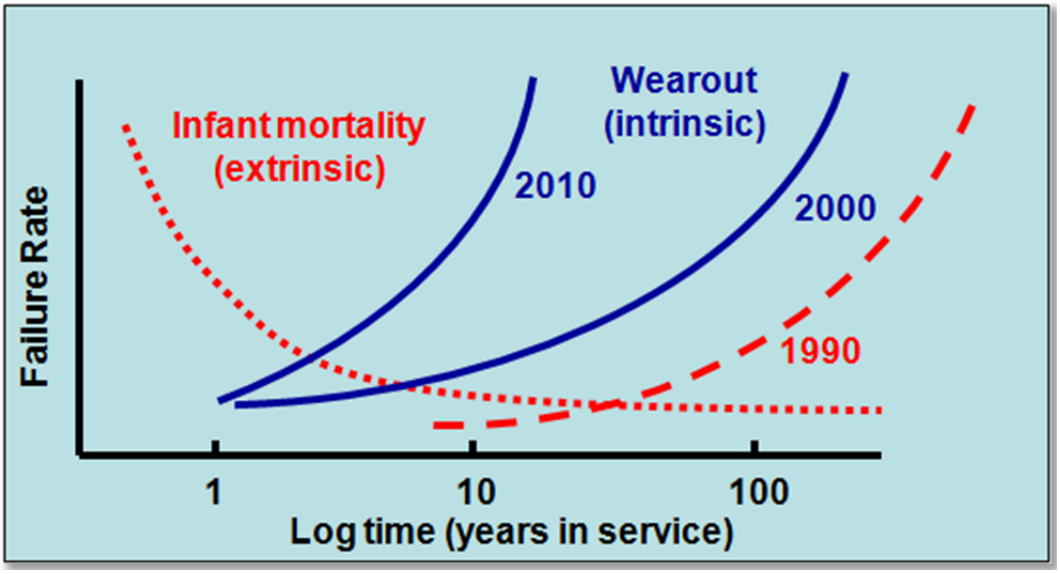

Figure 1. Generational product failure rates versus time in service, from [2].

As a result, the IC design engineer must now also be knowledgeable of device reliability, how devices degrade over time under specified operating conditions, and use this knowledge to design ICs and systems that meet product performance requirements while reliably meeting the specified service lifetime objective. Radiation effects and extended operating conditions commonplace in military and aerospace systems exacerbate this challenge. Published works directed toward the design community are beginning to surface with topics related to reliability-aware design [3], [4], [5], [6] that address emerging device and system reliability concerns; however, for the design engineer, there is very little in the literature that addresses both the emerging reliability concerns and radiation effects.

1. AMS Design for Space

AMS circuit designs, such as the pipelined analog-to-digital converter (ADC) identified in Figure 2, are fundamental to the operation of satellite communications (SATCOM) systems such as those employed by the military and the aerospace communities.

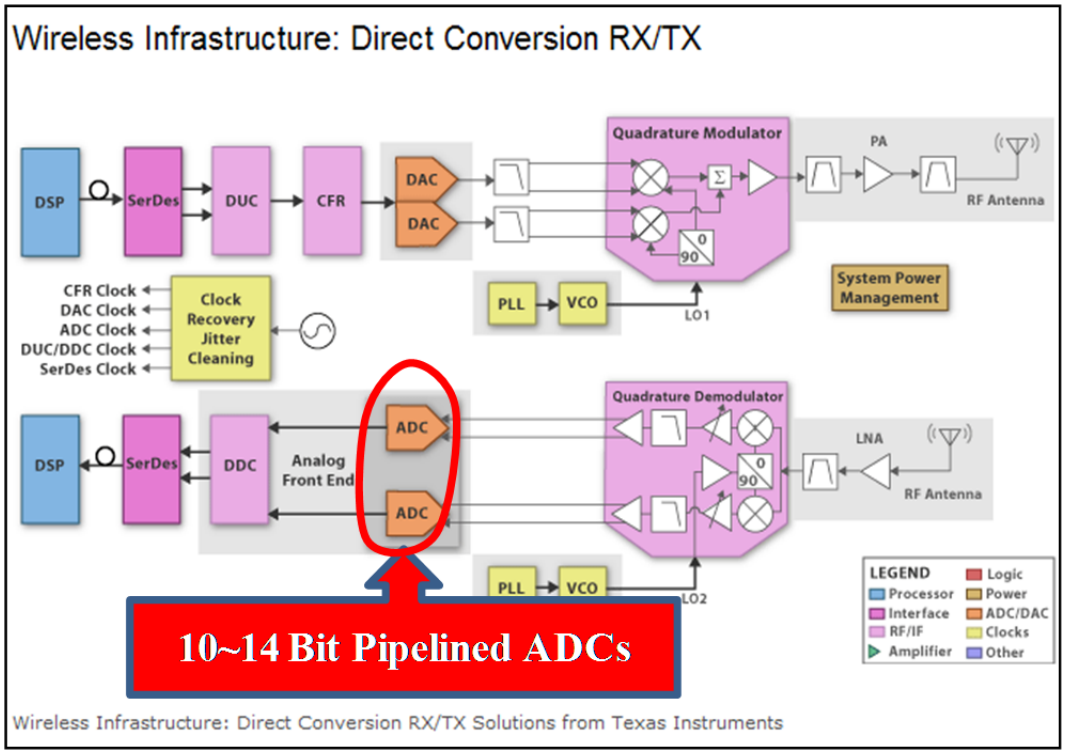

Figure 2. Wireless transceiver typical of those found in SATCOM systems.

Though the operation of the ADC is beyond the scope of this dissertation, the complexity of such a circuit (and system), as demonstrated in the block diagram of Figure 3, is useful in illustrating the magnitude of the challenge the designer faces in reliably designing products for military and space applications as each block of the ADC system has its own set of, often competing, design challenges. Yet, each of the system blocks have one fundamental device in common that is central to the topic of this dissertation, the metal-oxide semiconductor field-effect transistor, or MOSFET, manufactured in a commercial semiconductor fabrication process. In the sections that follow, the three foremost considerations influencing the design process, for the military and aerospace communities, are briefly discussed leading up to the topic of this dissertation.

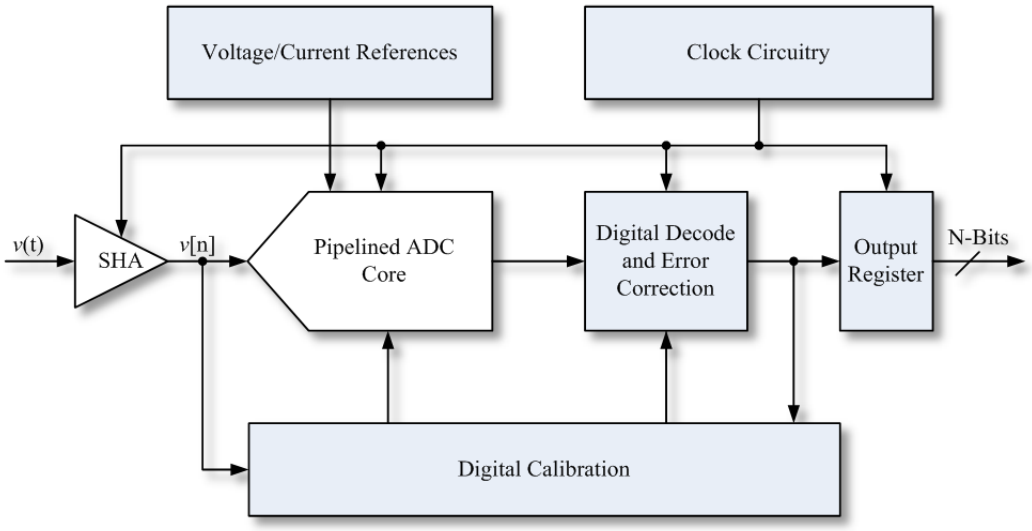

Figure 3. Functional block diagram of the ADC system identified in Figure 2.

a. Semiconductor Fabrication Process Variation

For the design engineer architecting such a system, not only must the system work as specified over the projected maximum operating conditions (temperature and voltage) it must do so taking into consideration semiconductor fabrication process variation which results in the key parameter variation in the electrical characteristics of the MOSFET and other electrical components available to the designer. This variation is typically random in nature and exhibits a Gaussian distribution and is well characterized by the semiconductor foundry—however, the details of the distribution (other than the nominal, upper, and lower boundaries) may not be shared with the design engineer.

b. Space Environment

In product development for the space environment, the designer must not only take into consideration the effects of ionizing radiation incurred over the product lifetime, or total ionizing dose (TID) irradiation that also contribute to the variation of key electrical parameters of the MOSFET; but, also take into consideration radiation induced single events effects (SEE) that can cause temporary system upset resulting in corrupted data, or possibly induce catastrophic and permanent circuit failure due to energetic particles such as high-energy electrons and protons encountered in Earth orbit.

The electron and proton belts containing the energetic particles are depicted in the diagram of Figure 4 illustrating the radiation environment about the Earth.

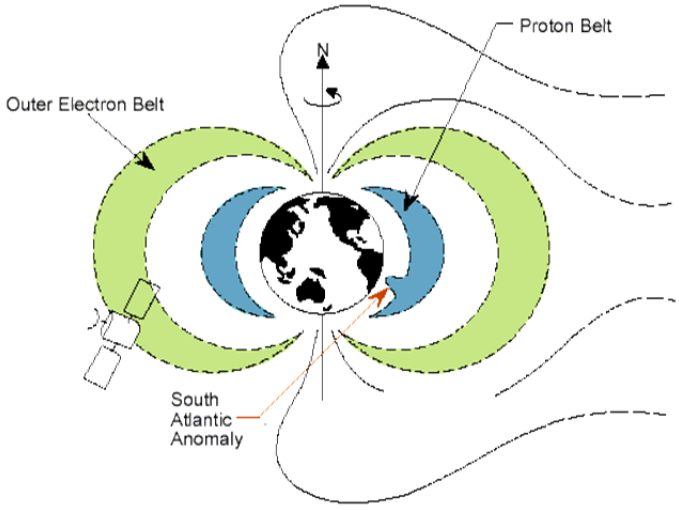

Figure 4. Trapped particle radiation belts around the Earth, from [7].

c. Device Reliability

To add to the design challenge, the designer must also consider the device reliability effects of hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), negative, and positive bias temperature instability (NBTI and PBTI respectively) on the MOSFET. The effect of NBTI on the p-channel MOSFET is studied exclusively in this dissertation. For the interested reader, several good books exist that, in addition to NBTI, cover HCI, TDDB, and other device reliability issues [8], [9], [10], [11], [12] from both the device physicist's and reliability engineer's perspective.

d. Combined Effects

The combined device reliability and radiation effects can lead to significant degradation in system performance and, if left unmitigated, premature and catastrophic system failure. Unfortunately, the combined interaction between device reliability effects and radiation effects is often not well documented or well understood. As a result, this topic is beginning to get the attention of the military and aerospace communities precisely because of the lack of data.

2. PMOS NBTI and Total Ionizing Dose Irradiation

Of the previously identified reliability effects, NBTI in p-channel MOSFETs, or PMOS devices, is widely accepted as the foremost concern within the reliability community. This is due to the significant effect NBTI has on the lifetime of PMOS devices in modern and state-of-the-art CMOS semiconductor fabrication processes. Even though significant research has been performed on the topic, the physical mechanisms responsible for PMOS NBTI have yet to be conclusively identified. Ultimately, while significant research has been performed over the years on TID irradiation, there has been little research reported in the literature on the combined effects of TID irradiation and NBTI on PMOS devices—and thus the topic of this dissertation: "PMOS NBTI in an Ionizing Radiation Environment."

B. BACKGROUND ON NBTI AND TID RADIATION

In this section, the evolution of NBTI is presented with the goal of demonstrating why it has become the foremost reliability issue in modern semiconductor processes. This is followed by a discussion on TID irradiation and why it is used to characterize device (transistors, circuits, and systems) performance in a space irradiation environment. A more quantitative treatment of the operation of the PMOS transistor, NBTI, and TID irradiation is presented in Chapter II.

1. Negative Bias Temperature Instability

To follow, the effects and history of NBTI are presented. Then, a discussion of why NBTI has become the foremost reliability issue is given. The discussion then concludes with the controversy surrounding the competing theories of the physical mechanisms responsible for NBTI.

a. What is NBTI?

NBTI is a PMOS transistor wearout mechanism characterized by the degradation of several key electrical parameters as a result of the device operating at an elevated temperature while a negative bias voltage is applied to the gate terminal of the device [9]. NBTI worsens with time (stress duration) and is a strongly influenced by

operating conditions such as the increased electric fields and operating temperatures inherent in modern semiconductor technologies. NBTI is also a well-documented recoverable phenomenon by which some the degradation incurred during the stress regime recovers once the stress is removed; hence the "instability" term in NBTI. Figure 5 demonstrates the bias condition of the PMOS transistor to induce NBTI.

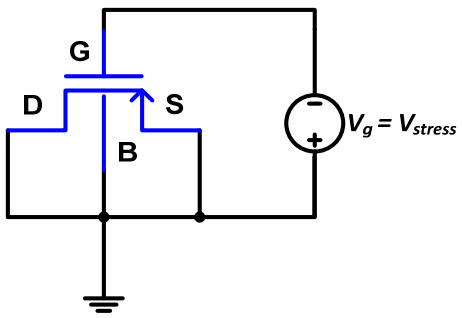

Figure 5. A PMOS transistor under negative bias conditions.

The key electrical parameters of the PMOS transistor affected by NBTI are the device threshold voltage V_T, transconductance g_m, effective mobility μ_{eff}, and drive current I_{DS}. The aforementioned MOSFET device parameters are defined and discussed in greater detail in the chapters to follow.

b. History of NBTI

The NBTI phenomenon has been known for decades and was first observed in the 1960s during the CMOS process development. It was addressed by annealing the insulating SiO_2 gate dielectric (or commonly referred to as gate oxide) in hydrogen prior to depositing the gate polysilicon layer to tie up dangling bonds at the Si-SiO_2 interface [10]. In the 1990s, NBTI resurfaced as a result of the scaling of the thickness of the gate dielectrics without reducing the device operating voltage. This resulted in an increase in the applied electric field E_{OX} across the device gate oxide approaching 10 MV/cm. However, it was not until the early 2000s that NBTI became an emerging reliability concern when it was observed that device lifetimes were becoming significantly reduced. This NBTI induced reduction in device lifetime was due primarily to continued scaling of the gate oxides and the introduction of nitrogen during the

transition from SiO_2 to SiON gate dielectrics. Though the introduction of nitrogen into the gate oxide addressed issues related to gate oxide scaling (gate leakage currents, dielectric breakdown, and boron penetration from the gate) it also increased the device vulnerability to NBTI as nitrided oxides were more susceptible to charge trapping [9], [13].

It was not until the mid-2000s that NBTI was to become the dominate reliability concern in the semiconductor fabrication industry. This was due to the introduction of high-k dielectrics to further reduce gate leakage currents while improving transistor drive strength. From the mid-2000s to the present, PMOS NBTI has become, and is, the foremost reliability concern in the semiconductor industry.

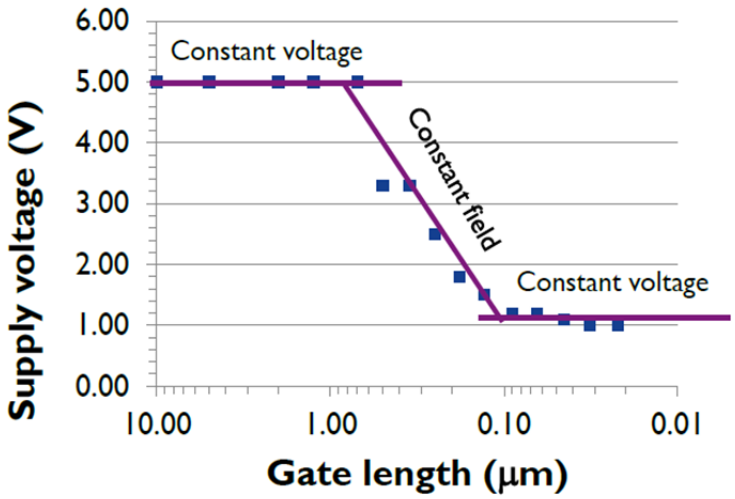

Figure 6. Device versus supply voltage scaling, from [4].

Figure 6 demonstrates the industry's device and voltage scaling trends over the last thirty or so years. What is implied here is that as the transistor gate length is scaled, so does the gate oxide thickness. The far-left "Constant voltage" region corresponds to the oxide thickness scaling era of the late-1980s to the mid-1990s in which oxide scaling continued until the industry approached the 10 MV/cm E_{OX} dielectric breakdown limit for SiO_2. The "Constant field" region corresponds to the gate oxide and supply voltage scaling era that began in the mid-1990s and kept the industry near the SiO_2 breakdown limit until the mid-2000s. Device operation near this oxide-breakdown

limit was maintained until another fundamental limit was reached, the 1-V supply limit. This limit, a result of process variation in the engineering of transistor threshold voltage V_T, was reached in the mid-2000s and is identified by the "Constant voltage" region on the right side of the graph. This era is also marked by the fundamental SiO_2 gate oxide scaling limit of 1 nm, beyond which gate electron tunneling currents become a significant contribution to device power dissipation. Hence the need to introduce new materials such as nitrogen and high-k dielectrics into the gate-oxide material system to keep the scaling trend going.

c. Why NBTI Has Become the Foremost Reliability Issue

The prior historical discussion provided the relative importance of NBTI to device and supply scaling events in the semiconductor industry; nevertheless, lacks some specifics as to why the addition of nitrogen to the gate oxide, and the introduction of high-k dielectrics, such as HfO_2, have resulted in a significant increase in the susceptibility of PMOS devices to NBTI. For decades SiO_2 had proved to be a near ideal material for the gate oxide dielectrics used in CMOS processes. It was, compared to other material systems, an extremely reliable material and nearly perfect insulator with desirable electrical properties (high bandgap material) that made it most suitable for the fabrication of CMOS semiconductor devices. However, device scaling demands exceeded what SiO_2 could provide.

As the semiconductor industry moved to address the limitations of the SiO_2 and take steps to mitigate other device scaling roadblocks, four major developments have contributed to the rise of NBTI:

- E_{OX} approaching the 10 MV/cm limit of SiO_2
- Changes in the gate-poly material system to reduce short-channel effects, (specifically, the introduction of boron)
- The introduction of nitrogen into the SiO_2 gate-dielectric system to reduce boron penetration into the gate dielectric, also reduced the gate-oxide resilience to NBTI
- The subsequent introduction of high-k dielectrics which are less resilient to NBTI.

These developments are discussed in greater detail, where relevant, in the chapters to follow.

d. Competing Theories

To complicate the landscape further, the debate regarding the physical mechanisms behind NBTI in PMOS devices remains hotly contested and to this day unsettled. There are two main competing theories that attempt to account for the NBTI phenomenon. The first and long-standing theory until recently is the reaction-diffusion (R-D) model involving hydrogen transport from the Si-SiO_2 interface into the gate-oxide espoused by Alam et al. [14] as shown in Figure 7. The second and more recent theory offered by Lenahan et al., and to a first order substantiates, the theory of hydrogen transport as described by the R-D model does not account for the NBTI phenomenon [15]. This second model has been referred to as the switching oxide trap model.

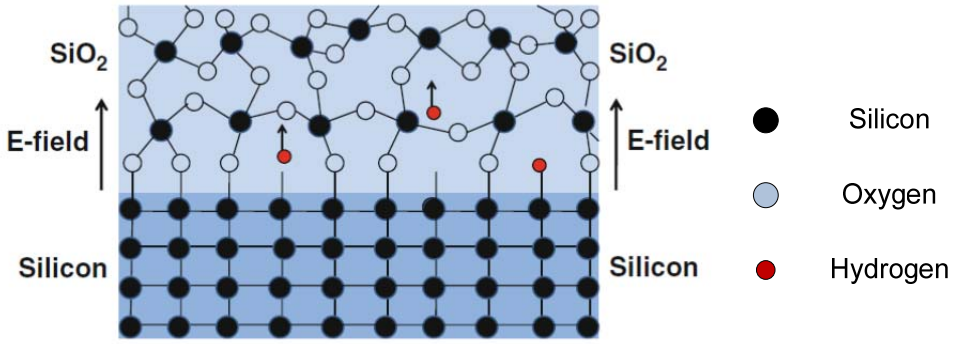

Figure 7. Cartoon depicting hydrogen transport attributed to R-D theory, from [12].

The latter model is compelling as it accounts for what is called the instantaneous recovery component observed in NBTI; whereas, the R-D model throughout its existence has failed to accurately account for this component.

As a final note, regardless of the material system (SiO_2, SiON, or high-k) the debate over NBTI remains unsettled. The only issue that has been settled is that with device scaling NBTI has worsened and with the introduction of nitrogen and high-k dielectrics the reliability situation of PMOS devices due to NBTI has been exacerbated.

2. Ionizing Radiation

Though there are several types of radiation encountered in the space environment, the resulting damage they cause can be generalized into three groups [16]; *charge trapping* in the oxide regions of semiconductor, *displacement damage* throughout the semiconductor material; and, *single-event effects* (SEE). SEE, which results in logic upsets, is caused by galactic cosmic rays and Van Allen belt protons that produce ionizing tracks in the proximity of transistors. Displacement damage, the physical displacement of lattice atoms, is primarily due to neutron and proton flux events in the radiation belts about the Earth. And, charge trapping is a result of ionizing radiation in the form of energetic charged particles such as electrons, protons, ionized atoms, and photons (gamma-rays and X-rays). In this dissertation ionizing radiation and total dose effects as a result of gamma-rays are of greatest interest as the charge trapping in the oxide and interface regions of the CMOS device is the most relevant to CMOS device reliability.

a. TID Radiation Effects

Ionizing radiation and TID effects cause charge trapping in the gate dielectric and isolating oxide regions of the CMOS device and charge trapping in the field oxide regions between devices. When energetic particles encounter these regions of the semiconductor, electron-hole pairs are created. If the electron-hole pairs are under the influence of an electric field, the electrons being highly mobile compared to holes get swept up in the electric field and drift away leaving the less mobile positively charged hole behind in the oxide.

To illustrate this phenomenon, the n-channel MOSFET cross section of Figure 8 demonstrates positive charge trapping in the buried oxide (BOX) region of the transistor as a result of being exposed to ionizing radiation [17].

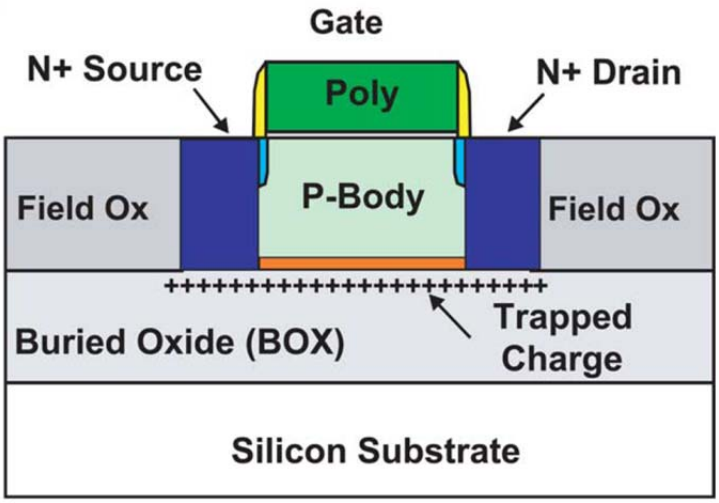

Figure 8. Cross section of an NMOS device with trapped charge after being irradiated, from [17].

In this case, the trapped positive charge has caused a back-gate channel to form creating a conducting channel from source to drain. This conduction can now take place regardless of the voltage applied to the gate terminal. The accumulation of oxide charge in the field oxide regions can cause loss of isolation between adjacent devices.

When this accumulation occurs in the device gate oxide and Si-SiO_2 interface, as is the case for the research carried out in this dissertation on p-channel MOSFETs, many of the same degradation, or shifts, in the key electrical parameters as was described for NBTI can take place resulting in changes to the device V_T, g_m, μ_{eff}, and I_{DS} parameters; albeit at the hands of a different physical catalyst—ionizing radiation versus NBTI temperature and voltage stresses.

b. Ionizing Radiation in State-of-the-Art CMOS Processes

It is commonly accepted that TID effects in state-of-the-art semiconductor processes will be minimal. This is due to the smaller gate-oxide volumes and cross-sections (i.e., smaller gate area of the transistor) that are a result of the course of device scaling. It is also surmised that the increased gate leakage currents in advanced technology nodes has a larger effect, to many orders of magnitude, than those as a result of ionizing radiation. Though the trend of reduced total dose effects [2], [10] as a

function of advancing technology node supports this assertion there have also been reports of enhanced TID effects due to the increase in the number interconnect layers inherent in state-of-the-art processes [18], [19]. Furthermore, high-k dielectrics, used to minimize gate tunneling currents by allowing thicker gate oxides to be manufactured while maintaining or improving the transistors drive strength, have larger gate-oxide volumes that could give rise to increased charge trapping in the gate oxide as a result of ionizing radiation. To date, very little has been published on TID effects in state-of-the-art semiconductor processes.

3. Combined Effects

As was previously stated, ionizing radiation and NBTI affect the same device parameters though parametric shifts are due to different physical mechanisms. Whereas the parametric shifts attributed to NBTI are a result of enhanced electric fields and elevated temperatures encountered in typical operating conditions; for TID effects, the parametric shifts are due primarily to interface charge trapping at the Si-SiO_2 interface and oxide trapping in the gate dielectric.

Similar to the case of very little being reported on TID effects in state-of-the-art processes, very little has been published in the literature regarding the combined NBTI and TID effects, with the exception of the work performed by Zhou [20], which examined developmental high-k capacitor structures manufactured in a research environment and concluded that, in the case of early high-k dielectric structures, the combined effects of NBTI stressing and ionizing irradiation was worse than the sum of the effects. Since this early (circa 2005) high-k research, the material system has been refined and improved results reported [21]. However, follow-on research on commercially available CMOS processes has not been performed thus begging the fundamental question: is NBTI enhanced in the space environment due to ionizing radiation; and, if so, to what extent and why?

C. THE PROPOSED RESEARCH AND SIGNIFICANT CONTRIBUTIONS

In this section, the research proposed and performed, and the resulting significant contributions made by this research are presented.

1. Research Proposal

The goal of this dissertation research was to analyze the effect of ionizing radiation on the reliability concern of NBTI on PMOS devices fabricated in modern and state-of-the-art semiconductor processes suitable for AMS design; and, to put forth a model accounting for the observed effects. This research was performed on PMOS devices fabricated in 130 nm CMOS process incorporating nitrogen into the transistor gate dielectric—devices that are technologically relevant, and of interest, to the military and aerospace communities. The cross-section of the p-channel MOSFET is illustrated in Figure 9 and discussed in greater detail in Chapter II.

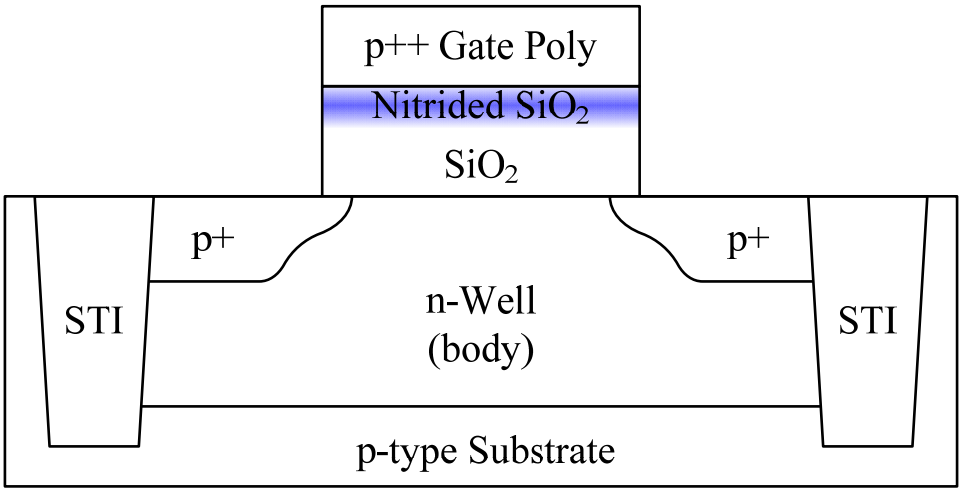

Figure 9. Cross-Section of the PMOS transistor.

In order to assess the effect of ionizing radiation on NBTI, three potential resulting outcomes were presumed possible: 1) Ionizing radiation does not affect PMOS NBTI; 2) ionizing radiation adversely affects PMOS NBTI; and, 3) ionizing radiation favorably affects PMOS NBTI. These assumed outcomes, a result of a device being exposed to ionizing radiation either prior to or during a NBTI producing bias and temperature stress, formed the basis for this research and how the research experiments would be conducted.

If observed, the first outcome would indicate that ionizing radiation is not an acceleration factor for NBTI. If ionizing radiation has an effect on the device, it is

separate of the NBTI effect and device degradation is additive, or a superposition of effects, which could suggest separate, uncorrelated, physical mechanisms at work.

If the second outcome were observed, this could suggest a synergistic effect between ionizing radiation and NBTI in which ionizing radiation is an accelerating factor for NBTI; whereby, NBTI (in addition to being a function of temperature, stress duration, and electric field strength) would also be a function of either TID or dose rate. If in the second outcome it were determined synergistic effects were strongly correlated to TID, then it could be inferred that the degradation, or breakdown of the material system, provides an opportunistic condition for NBTI. However, if the second outcome were discovered to be dose rate dependent, then the dose rate dependent dynamic processes (electron-hole, or *e-h*, production) could strongly influence the progression of NBTI—for better or for worse.

This leads to the third outcome; if observed, a particular dose rate could be responsible for retarding the progression of NBTI by creating a condition in which one of the reported physical mechanisms responsible for NBTI was impeded. However, if the improvement in the NBTI condition were TID dependent, then it could be inferred that by pre-irradiating the PMOS device that a hardening process has occurred which provides the device some immunity to NBTI.

A detailed experimental approach for investigating the potential outcomes are given in Chapter III; which is then followed by the presentation in Chapter IV of the observed experimental outcomes of the experiments performed preparing the reader for the combined effects results and analysis discussion of Chapter V.

In Chapter V, based on an analysis of the experimental data, and what has been reported in the literature, a model is developed that accounts for the combined effects of ionizing radiation and NBTI in PMOS devices.

Concluding with Chapter VI, we give a summary of the research performed and results obtained. This is followed a discussion of opportunities for further research such as extending experiments presented in this dissertation to semiconductor fabrication processes down to 32 nm and below.

2. Significant Contributions

a. Combined and Synergistic Effects Testing

There are a number of significant contributions that add to the body of scientific knowledge as a result of this research. These contributions include:

- The demonstration that ionizing radiation has a stress-bias dependent effect on PMOS NBTI
- A proposed NBTI characterization technique for evaluating the effects of ionizing radiation on PMOS NBTI
- Development of a model for ΔI_{ON} as a function of ΔV_T and $\Delta \mu_p$ that includes the combined effects of ionizing radiation and NBTI
- The development of a test and measurement system required to perform the experiments needed for the all of the above contributions

The first bullet is of interest to the reliability physics community and may spur follow-on research within that community toward resolving the hotly debated physical mechanisms responsible for NBTI. Furthermore, the knowledge that ionizing radiation may exacerbate PMOS NBTI is of immediate interest to the military and aerospace systems design communities.

The second bullet is also of interest to the reliability physics community as it provides a method for examining the combined effects of NBTI and ionizing radiation on PMOS NBTI. Moreover, combining the NBTI characterization standard and ionizing radiation gives reliability engineers tasked with evaluating and characterizing technologies targeting military and aerospace applications a method for evaluating the combined effects.

The third bullet is of interest to the design community. The model identifies a mathematical relationship between ionizing radiation and NBTI that can be developed further and applied to new and emerging material systems and technologies of interest to the military and aerospace communities.

The ability to do combined effects analysis under operationally relevant conditions has been gaining interest of late; therefore, the final bullet is of interest to

those wanting to perform combined effects analysis for the purpose of device, circuit, and system development, evaluation, and validation.

b. Publications Resulting from this Research

Technical publications resulting from this research include two poster manuscripts titled "PMOS NBTI analysis of a 45 nm CMOS-SOI Process with Nitrided Gate Dielectric" and "On the Device Response of a 45 nm PMOS Transistor to TID and NBTI Stresses" published in the proceedings of the 2012 IEEE International Integrated Reliability Workshop (IIRW) and the 2013 Government Microcircuit Application & Critical Technology (GOMACTech) conference respectively. In addition, journal manuscripts based on this research are currently being produced for submission to the IEEE publications related to device physics, reliability, and radiations effects. Titles of the manuscripts to be submitted include:

- The use of the NBTI Characterization Framework for Evaluating the Effects of Ionizing Radiation on NBTI
- The Dependence of PMOS NBTI on Ionizing Radiation
- The Effect of Ionizing Radiation on NBTI

D. CHAPTER CONCLUSION

In this introductory chapter, the motivation for this work, reliable AMS design for space, was presented followed by the overall challenges in accomplishing such a design. This discussion paved the way for the specific issue addressed in this dissertation, PMOS NBTI in an ionizing radiation environment. The proposed research and significant contributions section of this chapter outlined the organization of the work that follows and concluded with publications resulting from this work.

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II. MOSFET THRESHOLD VOLTAGE DEGRADATION MECHANISMS IN MODERN SEMICONDUCTOR TECHNOLOGIES

PMOS NBTI, whose physical mechanisms are not well understood, is the foremost reliability concern in the semiconductor industry today. Furthermore, the effect of ionizing radiation on PMOS NBTI has not been studied within the framework of NBTI characterization. The primary effect of PMOS NBTI and ionizing radiation on PMOS operation is the characteristic shift in the device threshold voltage. In this chapter, what is known about the material system being researched is presented. This is followed by a presentation of the MOSFET threshold voltage. After which, what is currently known about PMOS NBTI and ionizing radiation is presented emphasizing their effects on the device threshold voltage.

A. DEFINITION OF THE MATERIAL SYSTEM UNDER STUDY

The p-channel MOSFETs under study were manufactured on a commercially available 130 nm CMOS process. It is assumed that the material structure of the p-channel MOSFET is comprised of a heavily doped p-type polysilicon gate atop a SiO_2 gate dielectric grown on an n-type silicon body formed in a p-type silicon substrate. It is also assumed, due to the technology node, that an isolating region of shallow-trench isolation (STI) comprised of SiO_2 was incorporated for the purpose of device-to-device electrical isolation. The source and drain regions are assumed to be doped p-type silicon. The physical gate-dielectric thickness t_{phy} is 2.2 nm and the device width and length parameters, W and L, are 5 and 0.12 μm, respectively. The cutaway drawing of Figure 10 illustrates the as-described features of the p-channel MOSFET.

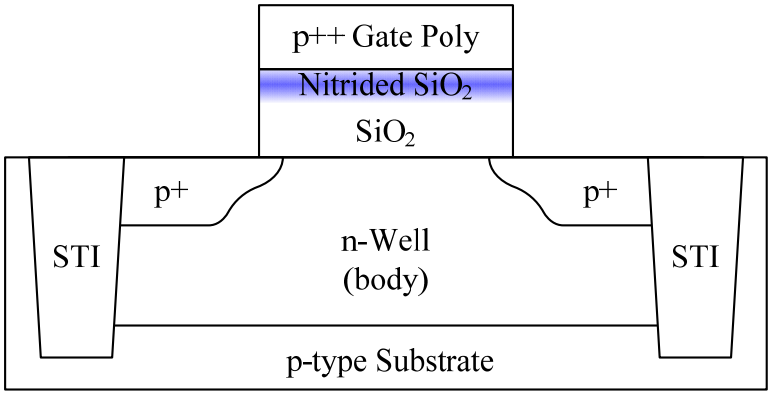

Figure 10. P-Channel MOSFET cross-section, gate-oxide thickness not to scale.

Incorporation of nitrogen, or nitrogen engineering, into the gate stack to form a nitrided-SiO_2 gate dielectric is likely. The inclusion of nitrogen into the gate dielectric prevents boron penetration into the gate oxide from the heavily doped polysilicon gate. Toward this goal, it is common for nitrogen to exist as a nitride top layer forming SiO_xN_y thereby isolating the gate-poly from the SiO_2. There could also be a nitride layer at the Si-SiO_2 interface for the purpose of passivating interfacial dangling Si bonds. Furthermore, due to its ultra-thin nature, the gate dielectric could consist entirely of SiO_xN_y. In addition to blocking boron diffusion and shoring up interfacial dangling bonds, the incorporation of nitrogen has the effect of slightly raising the gate-oxide dielectric constant *k*. Assuming nitrogen is present in the gate stack of these devices, the per cent concentration, its distribution within the oxide, and the process by which it was incorporated is not known; however, in experimental devices, device reliability has shown sensitivity to these manufacturing factors, for both irradiation and NBTI.

B. MOSFET THRESHOLD VOLTAGE, V_T

The MOSFET threshold voltage V_T is defined as the applied V_{GS} sufficient to cause channel inversion thus allowing current to flow from the source to the drain terminals. Physically, this is the condition for which the carrier type in the channel between the source and drain of the transistor at the oxide-semiconductor interface is equal in density and opposite in charge to that of the native carrier type under equilibrium conditions as illustrated in Figure 11.

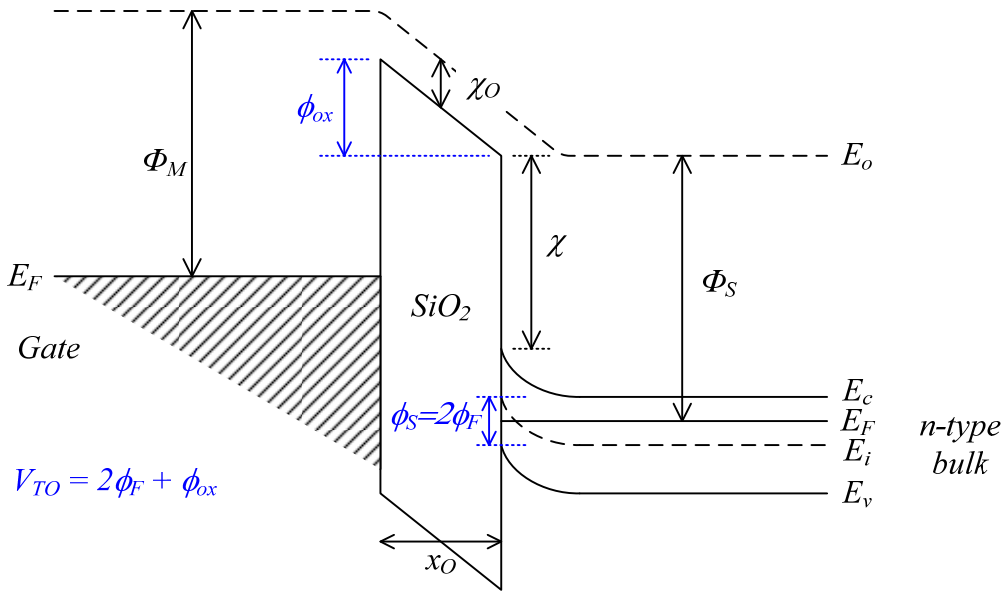

Figure 11. Energy band diagram for a PMOS device at the onset of inversion.

The onset condition whereby the transistor is capable of conducting current from source to drain occurs when $V_{GS} = V_T$. For the transistor channel to conduct appreciable current, V_{GS} must be greater than V_T, as demonstrated in the plot of Figure 12 where the x-intercept of the linear extrapolation of I_{DS} approximates V_T.

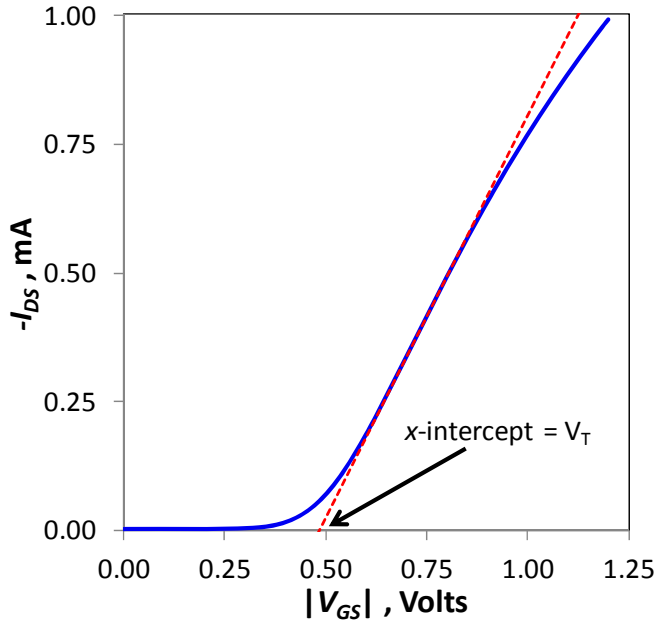

Figure 12. PMOS I_{DS}-V_{GS} characteristic curve with V_T.

In terms of voltage drops across the device semiconductor and gate-oxide regions, V_{GS} can be represented by

$$V_{GS} = \phi_S + \phi_{ox}. \tag{2.1}$$

For the case in which $V_{GS} = V_{TO}$ where V_{TO} is the ideal MOSFET threshold voltage representation of V_T absent work function and oxide charge effects, V_{TO} is given by

$$V_{TO} = 2\phi_F + \phi_{ox}, \text{ where} \tag{2.2}$$

$$\phi_F = \frac{1}{q}\left[E_{i(Bulk)} - E_F \right]. \tag{2.3}$$

The Fermi potential ϕ_F is related to the impurity dopant potential in *n*-type bulk or substrate region of the PMOS transistor and is given by [10]

$$\phi_F = -\frac{kT}{q}\ln(N_D / n_i) \quad \text{n-type semiconductor.} \tag{2.4}$$

The oxide potential, ϕ_{ox}, is the gate to oxide-semiconductor interface potential and is given by

$$\phi_{ox} = \frac{K_S}{K_O} x_O \sqrt{\frac{2qN_D(-\phi_S)}{K_S \varepsilon_O}} \text{ where } \phi_S = 2\phi_F \text{ when } V_{GS} = V_{TO}, \tag{2.5}$$

where ϕ_S is referred to as the surface potential. K_S and K_O are the dielectric constants of the silicon and gate-oxide (SiO_2) materials respectively, and x_O is the thickness of the gate-oxide layer. Figure 11 represents the ideal energy band diagram for a PMOS device at the onset of inversion.

E_O is the energy required by an electron to completely free itself from the material; this energy level is referred to as the vacuum level. The work functions of the gate material and the semiconductor are given by, Φ_M and Φ_S respectively and χ is the electron affinity denoting the energy barrier at the surface of the Si-SiO_2 interface. The Φ_M *and* χ parameters are fixed, material-property dependent, values and Φ_S is a function of the channel doping.

In our discussion thus far, Equation (2.2) represents the ideal threshold voltage equation which makes two assumptions. First, Φ_M and Φ_S are equal in value when in fact a mismatch exists. Secondly, and more importantly, the oxide charge effects in the gate oxide and at the semiconductor-oxide (Si-SiO_2) interface are neglected. In reality, the work function mismatch contributes a small and predictable ϕ_{MS} potential term. However, the oxide charge effects (oxide and interface traps, mobile ions and fixed charges) can contribute to significant voltage shifts and instabilities in V_T [10]. Taken collectively, the oxide charge effects and ϕ_{MS} terms are referred to as the flatband voltage V_{FB} and when combined with Equation (2.2) yields the non-ideality inclusive threshold voltage V_T

$$V_T = V_{TO} + V_{FB}, \tag{2.6}$$

in which V_{TO} is the ideal threshold voltage given previously, and the V_{FB} is given by,

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_{ox}} - \frac{Q_M \gamma_M}{C_{ox}} - \frac{Q_{IT}(0)}{C_{ox}}, \tag{2.7}$$

in which the Q_F/C_{ox} term is attributed to the voltage shift due to oxide fixed charge. The $Q_M\gamma_M/C_{ox}$ term accounts for the voltage shift due to mobile ions, and the $Q_{IT}(\phi_S)/C_{ox}$ term accounts for the voltage shift due to interfacial traps. The γ_M term is a coefficient normalized to the oxide thickness and represents the centroid of the mobile ions located within the oxide.

The fixed oxide charge is suspected to be due to excess un-reacted ionic silicon at the Si-SiO_2 interface upon the abrupt termination of the oxidation process. This leads to a positive fixed charge near the Si-SiO_2 interface which lowers the transistors threshold voltage. The fixed charge is not a function of oxide thickness, semiconductor impurity concentration or impurity type but varies with the surface orientation of the Si substrate. The conditions upon which the oxidation process terminates have a significant impact on the number of fixed charges.

Mobile ions are a result of contaminates left behind or finding their way in the oxide as part of the fabrication process. Though fabrication techniques have been introduced to eliminate or trap most of the mobile ions during the fabrication process,

they still exist. The presence of the mobile ion has the effect of contributing to bias instability of the transistor.

Interface charge traps N_{IT} take place at the Si-SiO_2 interface and are primarily a result of incomplete, or dangling, Si bonds occurring during the SiO_2 growth phase. Most of the interfacial silicon bonds to oxygen and a small amount of silicon later bonds to hydrogen leaving the bond electrically inactive. However, the Si-H bonds can break under high electric-field conditions allowing the hydrogen to migrate leaving surface states which in turn introduce allowed energy levels within the forbidden gap of the semiconductor creating trap centers. These interface traps contribute to surface potential dependent threshold voltage shifts and degradation in the devices transconductance.

Not given in Equation (2.7) but also a potential source of threshold voltage shift is the oxide trap. Oxide charge traps N_{OT} are generally charge neutral defects in the oxide that have the potential to trap charge carriers once activated. When trapped carriers accumulate in the oxide (as a result of hot carrier injection or radiation), the effect is a shift in the transistors threshold voltage and, over time, a sufficient accumulation of trapped charge due to activated oxide trap centers can lead catastrophic transistor failure such as time-dependent dielectric breakdown, or TDDB.

C. PMOS NBTI

1. Introduction

The NBTI phenomenon has been know for decades and was first observed in the 1960s during early CMOS process development [10]. After process improvements diminished this effect, SiO_2 had proved to be a near ideal material for the gate oxide dielectrics used in CMOS processes. It was, compared to other material systems, an extremely reliable material and nearly perfect insulator with desirable electrical properties (high bandgap material) that was most suitable for the fabrication of CMOS semiconductor devices (high melting point; easily grown on Si with introduction of oxygen).

Eventually, device scaling demands exceeded what SiO_2 could provide. With gate-oxide thicknesses approaching 1 nm, gate leakage currents due to electron tunneling

became intolerable as a result of the corresponding and dramatic increase in device power dissipation. Though new material systems (SiO_xN_y followed by high-k) were introduced to address the gate leakage issue, due to the increased electric fields and operating temperatures that also came with scaling, they proved to be less reliable. As a result, over the past decade, NBTI in PMOS devices has become the dominate reliability concern in the semiconductor industry.

In the discussion that follows, the characteristics of NBTI will be presented, followed by the physical mechanisms behind NBTI. After which, the characteristic, or empirical, model that characterizes NBTI dependence on electric-field strength, temperature, and stress duration, is presented; concluding with a discussion of NBTI measurement techniques used to characterize the changes in the key electrical parameters of the PMOS transistor.

2. Characteristics of NBTI

NBTI, as primarily a PMOS transistor wearout mechanism, is characterized by the degradation of key electrical parameters resulting from the device operating at an elevated temperature while under a negative gate-bias voltage [9]. NBTI worsens with time (stress duration) and is strongly influenced by operating conditions such as the increased electric fields and operating temperatures inherent in modern semiconductor technologies. NBTI is also a well documented recoverable phenomenon where a significant portion of the degradation incurred during the stress regime recovers once the stress is removed; hence the "instability" term in NBTI. The key electrical parameters of the PMOS transistor that can be dynamically affected by NBTI are the device V_T, g_m, μ_{eff}, and I_{DS}. The PMOS transistor under DC stress bias condition required to induce NBTI is shown in Figure 13.

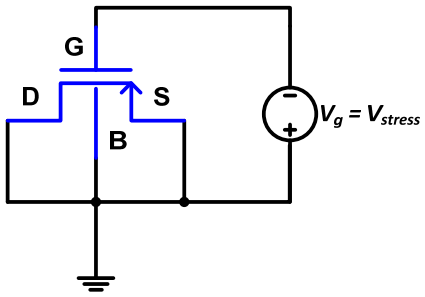

Figure 13. A PMOS transistor under negative DC bias stress to induce NBTI.

The two physical defects responsible for NBTI, an increase in the number of interface states and hole trapping near the interface, N_{IT} and N_{HT}, respectively are illustrated in Figure 14 [22]. As a result of bias and temperature stressing, the effect related to the oxide defect is positive charge trapping resulting from activated oxide hole traps which leads to a decrease of the V_T causing it to become more negative (increase in magnitude).

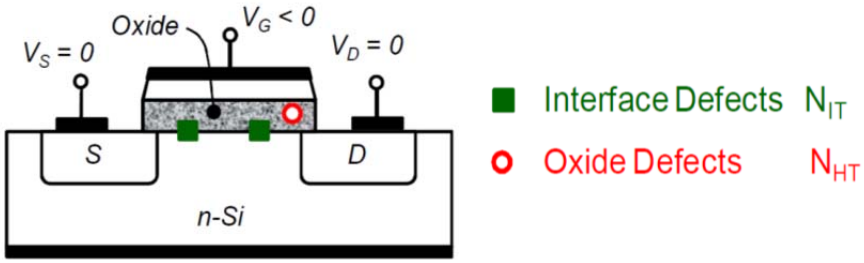

Figure 14. Cross-section showing location of interface and oxide trap centers, from [22].

The interface defects result in positive charge trapping at the interface leading to degradation of the μ_{eff} and contribute to a decrease (increase in magnitude) of the V_T. In terms of the V_{FB}, the change in the V_T can be written as

$$\Delta V_{FB} = -\left[\frac{Q_{IT}(\phi_s)}{C_{ox}} + \frac{Q_{HT}}{C_{ox}} + \frac{Q_{OT}}{C_{ox}}\right], \tag{2.8}$$

in which the N_{IT}, $N_{HT,}$ and assuming the existence an oxide trap component N_{OT}, are, respectively, responsible for the Q_{IT}, Q_{HT}, and the Q_{OT} terms. The normalized plot of Figure 15 illustrates the characteristic nature of the change in the V_T over time due to a constant DC stress on a linear and log-log scale.

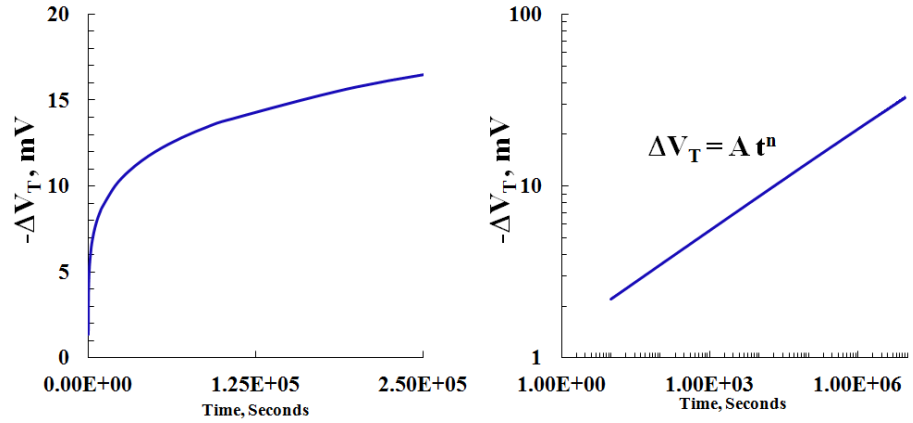

Figure 15. Characteristic ΔV_T curve for continuous DC stress.

The ΔV_T equation takes on the form

$$\Delta V_T = A\left(E_{ox}, T\right) \times t^n, \tag{2.9}$$

in which the pre-factor term $A(E_{ox},T)$ represents the electric field and temperature dependent parameters responsible for the V_T degradation due to NBTI. In the most current literature the power law exponent n has been reported as being approximately equal to 1/6.

The I_D-V_G curves of Figure 16 demonstrate the effect NBTI has on device characteristics, primarily a negative translation of the curves on the horizontal axis is an indication of positive charge trapping responsible for the negative shift in the V_T and a decrease in the device μ_{eff} as evidenced by the spreading out of the I_D-V_G curve.

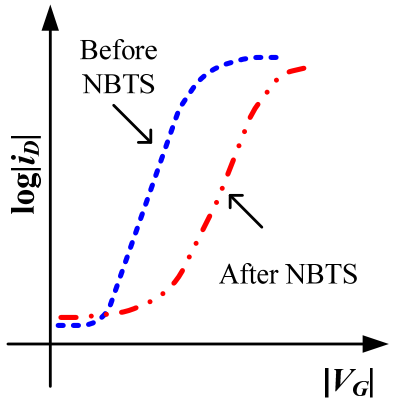

Figure 16. Plot of parametric degradation characteristic of NBTI.

In Figure 17, the separate contributions to ΔV_T by the interface states, hole trapping, and bulk-oxide trapping are shown, where the total contribution to ΔV_T is given by

$$\Delta V_T = \Delta V_{IT} + \Delta V_{HT} + \Delta V_{OT}, \tag{2.10}$$

which is consistent with Equation (2.8).

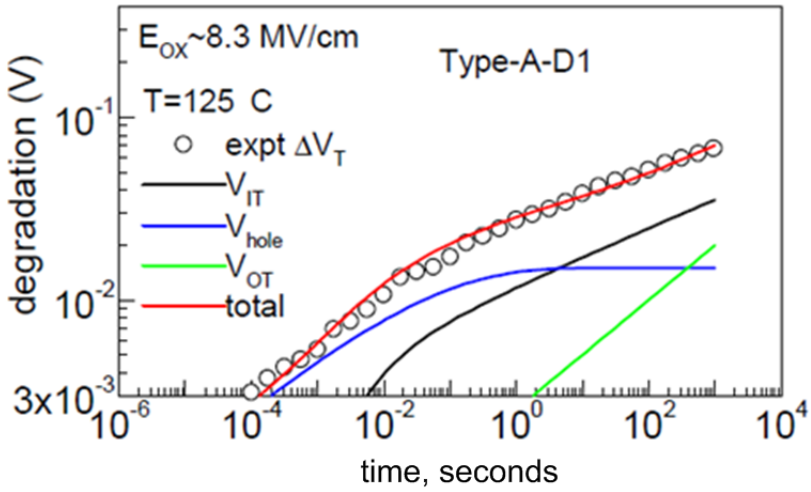

Figure 17. Time evolution of degradation due to NBTI, from [23].

From a temporal perspective, it is observed that the $\Delta V_{T\text{-}HT}$ process occurs first then saturates, which is then followed by the $\Delta V_{T\text{-}IT}$ and the subsequent $\Delta V_{T\text{-}OT}$ processes. According to Mahapatra et al. [23] the $\Delta V_{T\text{-}IT}$ component is attributable to, and thus modeled by, the R-D framework discussed in the following section regarding the physical mechanisms leading to NBTI.

Once the stress is applied, degradation in V_T as a function of time similar to that shown in Figure 15 is observed. However, once the stress is removed (within a second) a significant amount of recovery ($\Delta V_{T\text{-}REC}$) also occurs. The plots of Figure 18 provide a notional illustration of the recoverable nature of the NBTI phenomenon observed once the negative bias stress is removed. This NBTI recovery component is attributed to the near-instantaneous de-trapping of the oxide and bulk traps; the de-trapping of the interface states ($\Delta V_{T\text{-}nonREC}$) proceeds in a back diffusive process where hydrogen

dissociated from the interface during the stress cycle make their way back to the interface and re-passivate dangling bonds during the recovery phase over a much longer period [23].

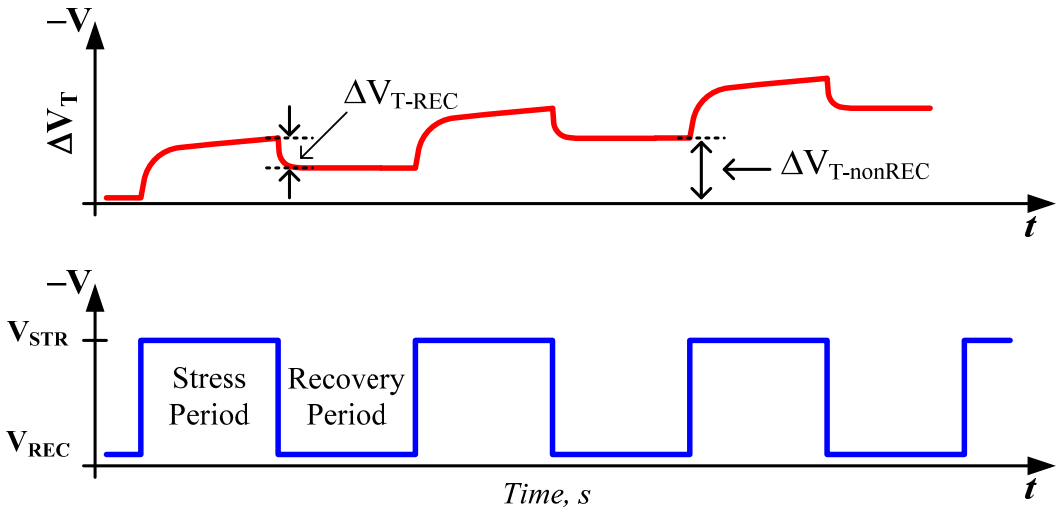

Figure 18. Stress induced NBTI with recoverable and permanent components of ΔV_T.

It should be noted that the recoverable component did not gain attention until the early-2000s when researchers were at odds with the seemingly disparate reporting of data obtained from similar technologies. As it turned out, the measured degradation in the threshold voltage was highly sensitive to the interval between stress removal and threshold voltage measurement. If the measurement cycle began too soon after the stress was removed, a portion of the fast-recovery component would corrupt a measurement intended to capture the long-term degradation of the device and thereby over reporting the amount of degradation. The interval between stress removal and measurement cycle, distinguishing between short-term (recoverable) and long-term (non-recoverable) components, is about one second. The fast-recovery component occurs practically instantaneously, on the order of $10^{-6} \sim 10^{-3}$ seconds. Whereas the long-term component exhibits recovery, but on a much longer time scale covering several decades; nearly imperceptible on the time scales used for the measurement period.

This realization spawned a great deal of interest in fully characterizing the NBTI phenomenon that eventually led to the current controversy surrounding NBTI. Is the long-standing R-D model valid for characterizing NBTI? It is not the author's intent to solve this controversy here; however, a review of the two competing theories in terms of the physical mechanism behind NBTI follows.

3. Physical Mechanisms of NBTI—Competing Hypotheses

The debate regarding the physical mechanisms behind NBTI in PMOS devices remains hotly contested and to this day unsettled. There are two main competing theories that attempt to account for the NBTI phenomenon.

The first and long-standing theory until recently is R-D model involving hydrogen disassociation (or depassivation) from the Si-SiO_2 interface and diffusion into the gate-oxide. The second model proposes, and to a first order substantiates, the theory that hydrogen transport as described by the R-D model does not adequately characterize the NBTI phenomenon [15]. This alternate model is referred to as a switched-trap model where hole tunneling across the interface and trap-switching to and from interface states to trap centers within the oxide occurs.

The latter model is compelling as it attempts to account for the instantaneous recovery component observed in NBTI; whereas, the R-D model throughout its existence has failed to account for this component. Neither model universally accounts for both the stress and relaxation phases of NBTI; however, what both models do is propose a physical-based hypothesis to explain the NBTI phenomena for both the stress and recovery phases based on empirical observations.

a. R-D Theory (Purdue and IIT)

The R-D model involving the disassociation of hydrogen from the Si-SiO_2 interface and diffusing into the gate oxide, first introduced by Jeppson in 1977 [24] and espoused primarily by Purdue University and the Indian Institute of Technology (IIT) is presented in Figure 19.

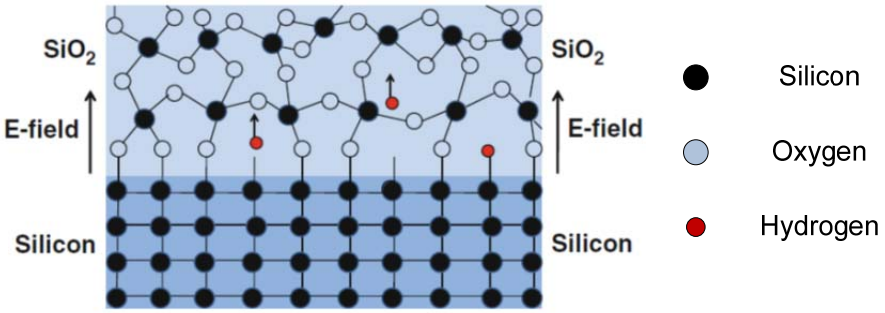

Figure 19. Cartoon from [12] depicting hydrogen transport attributed to R-D theory [14].

From Figure 19 it is observed that under negative bias a hydrogen atom dissociates from the Si-SiO_2 interface and diffuses into the SiO_2 leaving behind a dangling bond defect at the interface. This process can be represented by the electrochemical reaction [25]

$$Si-H \rightleftharpoons Si^{\bullet} + H_c + H_t \tag{2.11}$$

in which H_c is hydrogen in a mobile state and H_t is hydrogen in a trapped state. It is generally assumed in the R-D model that all dissociated H is available for diffusive transport, and therefore, $H_t = 0$. Furthermore, it is assumed the dissociated hydrogen quickly combines to become molecular H_2. In its formulation of the R-D model [14], interface state generation rate takes the form given by [25]

$$\frac{\partial N_{it}}{\partial t} = k_F\left(N_0 - N_{it}\right) - k_R N_{it} H_{it}^{\,1/a}. \tag{2.12}$$

N_{it} represents the density of the generated interface trap as a result of broken Si-H bonds. N_0 is the pre-stress number of passivated Si-H dangling bonds available to contribute to interface state generation. Dissociation and anneal rates for how fast the bonds break and anneal are given by k_F and k_R, respectively; these rates are dependent on the electric-field across the oxide and temperature. The number of unbroken Si-H bonds is given by the $N_0 - N_{it}$ term. $H_{it}^{\,1/a}$ represents the number of mobile hydrogen and the $1/a$ term gives the order of the hydrogen reaction. For H and H^+, $a = 1$; and, for H_2, $a = 2$, assuming once again, instantaneous conversion of $H \rightleftharpoons H_2$. Finally, it is assumed that at $t = 0$, $N_{it} = 0$; and, all N_{it} generated contribute equally to ΔV_T.

With the goal of demonstrating the contribution of $N_{it}(t)$ to ΔV_T, and following the logic in [14], an equation is derived for $\Delta V_T(t)$ in the form

$$\Delta V_T(t) = A(E_{ox}, T)\ t^n. \tag{2.13}$$

Beginning with Equation (2.12) and realizing the rate at which interface traps are being created is extremely slow (quasi-equilibrium state) and that the number of N_{it} created is only a small fraction of N_0, therefore

$$\frac{dN_{it}}{dt} \approx 0 \quad \text{and} \quad (N_0 - N_{it}) \approx N_0, \tag{2.14}$$

and as a result,

$$k_F N_0 \approx k_R N_{it} H_{it}^{1/2}. \tag{2.15}$$

Here it is assumed the exponent on H_{it} is $a = 2$ implicit in the k_R term.

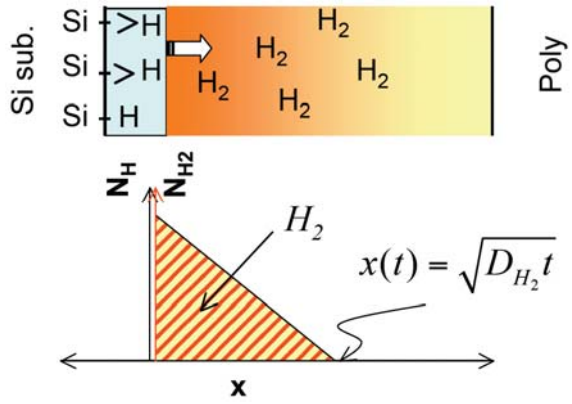

Figure 20. H_2 diffusion into oxide resulting from R-D process, from [14].

However, once free of the interface, the hydrogen reacts to form H_2. Whereas the concentration of H_2 in the oxide is given graphically in Figure 20, the area under the curve gives the number of interface traps as a function of time, $N_{it}(t)$. Mathematically, this can be represented by

$$N_{it}(t) = \frac{1}{2} H_{it} \sqrt{D_{H_2} t}, \tag{2.16}$$

in which $a = 1$ for the exponent term on H_{it} and the D_{H2} term is the diffusion rate, or diffusivity, for H_2 within the oxide. Solving for H_{it} in Equation (2.16) and substituting the result into Equation (2.15) yields

$$N_{it}^3(t) = \frac{1}{2}\left[\frac{k_F N_0}{k_R}\right]^2 \sqrt{D_{H_2} t}\ , \tag{2.17}$$

resulting in

$$N_{it}(t) = \left[\frac{k_F N_0 D_{H_2}^{1/4}}{\sqrt{2} k_R}\right]^{2/3} t^{1/6}. \tag{2.18}$$

From Equation (2.18) the interface trap generation takes on the generally accepted and often reported power-law time exponent of $n = 1/6$. Again, assuming all generated N_{it} contribute equally to the change in V_T, to obtain ΔV_T in the form of Equation (2.13) in terms of N_{it}, $qN_{it}(t)$ is substituted for Q_{IT}, which results in

$$\Delta V_T(t) = -\frac{qN_{it}(t)}{C_{ox}} \tag{2.19}$$

and

$$\Delta V_T(t) = -\frac{q}{C_{ox}}\left[\frac{k_F N_0 D_{H_2}^{1/4}}{\sqrt{2} k_R}\right]^{2/3} t^{1/6}. \tag{2.20}$$

Though the R-D model does a good job of predicting the power law exponent during stress, it fails to accurately predict or model the recovery (or relaxation) observed without significant modification to the model. One reason for this failure of the model is that it does not account for the fast recovery component of NBTI and furthermore it only predicts out to three or four decades the long-term recovery; whereas, the observed long-term recovery has been demonstrated to takes place over twelve decades as reported by Grasser et al. [25]. In defense of the R-D framework for modeling NBTI, Purdue and IIT account for this disparity by isolating the recovery contribution due to hole-trapping and oxide-trapping thereby introducing a modified R-D model in which hydrogen still plays the prominent role [22].

b. Reaction Dispersion Diffusion Model

Due to the inability to the R-D framework to accurately model the characteristic recovery phase of NBTI, the reaction dispersion-diffusion RDD model has gained some acceptance [25]. The RDD model makes use of the kinetic equation describing the reaction at the interface, repeated here for convenience:

$$\frac{\partial N_{it}}{\partial t} = k_F \left(N_0 - N_{it} \right) - k_R N_{it} H_{it}^{\,1/a}. \tag{2.21}$$

Whereas the R-D model of transport is drift-diffusion based on mobile hydrogen, $H_{it} = H_c$, the RDD model is trap-based in which $H_{it} = H_t$. As with the R-D model, the RDD model assumes the generation of N_{it} due to NBTI takes place slowly and, therefore, also assumes

$$\frac{\partial N_{it}}{\partial t} \approx 0. \tag{2.22}$$

The dispersive transport process for hydrogen [26], in which particles that have dissociated from the interface and residing in the conduction band E_c can fall into oxide traps and be subsequently reemitted into the conduction band, is illustrated in Figure 21.

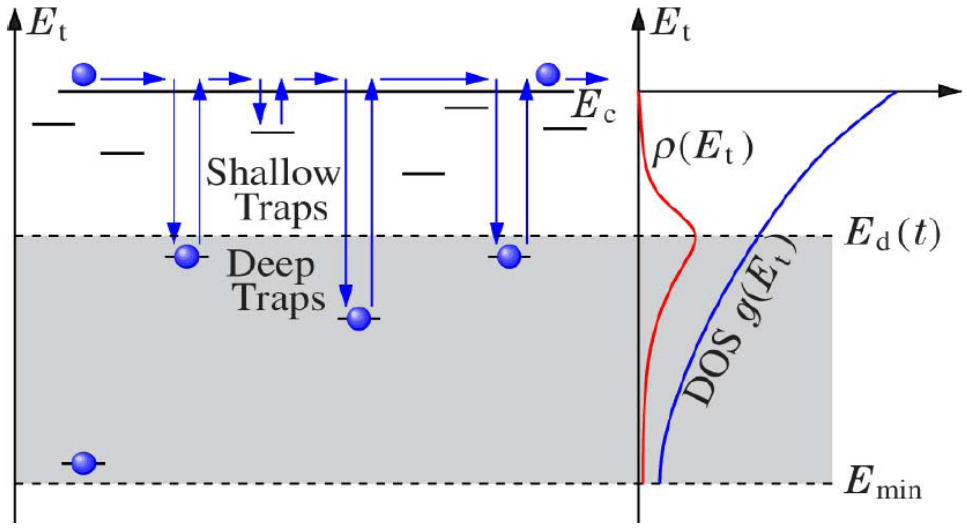

Figure 21. Dispersive Transport of hydrogen in an amorphous material, from [26].

Though most hydrogen resides in a trapped state, the frequency of reemission into the conduction band is higher for those in shallow traps, and lower for those in deep traps with the demarcation line between the two given by E_d. The hydrogen occupied trap density is given by $\rho(E_t)$. Also shown is the density of states $g(E_t)$ for traps within the forbidden gap. However, like the R-D model, this model fails to accurately describe the time-scale of the long-term recovery component [27].

c. Switched-Trap Model

Recently, a new model for describing NBTI has emerged and is gaining acceptance as an alternative to the R-D model. This model, referred to as the switching oxide trap model, or switched-trap model, has its origins from earlier work performed in the radiation effects community most notably by Lelis and Oldham [28]. In [28] Lelis presented the switched oxide trap model, or HDL (Harry Diamond Laboratory) model, that described the oxide charge trapping dynamics at suspected oxygen vacancies (E′-centers) in the SiO_2 near the Si-SiO_2 interface due to irradiation. Later, Conley et al. confirmed the E′-centers were in fact acting as the switched-trap centers [29]. In the work on radiation effects, researchers observed that interface state generation followed the oxide hole-trap process. However, it was not understood whether the two processes were independent of each other or coupled.

The switched-trap model of Figure 22 proposed by Goes et al. [30] adopts the HDL model for NBTI to describe the hole-trapping dynamics and extends it to include the interface state generation component as well. The significance of this model is that Goes proposed that the oxide hole trapping and interface state generation where two tightly coupled mechanisms that could be described as a two-stage process by which the oxide hole trap occurs first (at an E′-center) which then sets up the condition for the generation of an interface state (at the P_b-center).

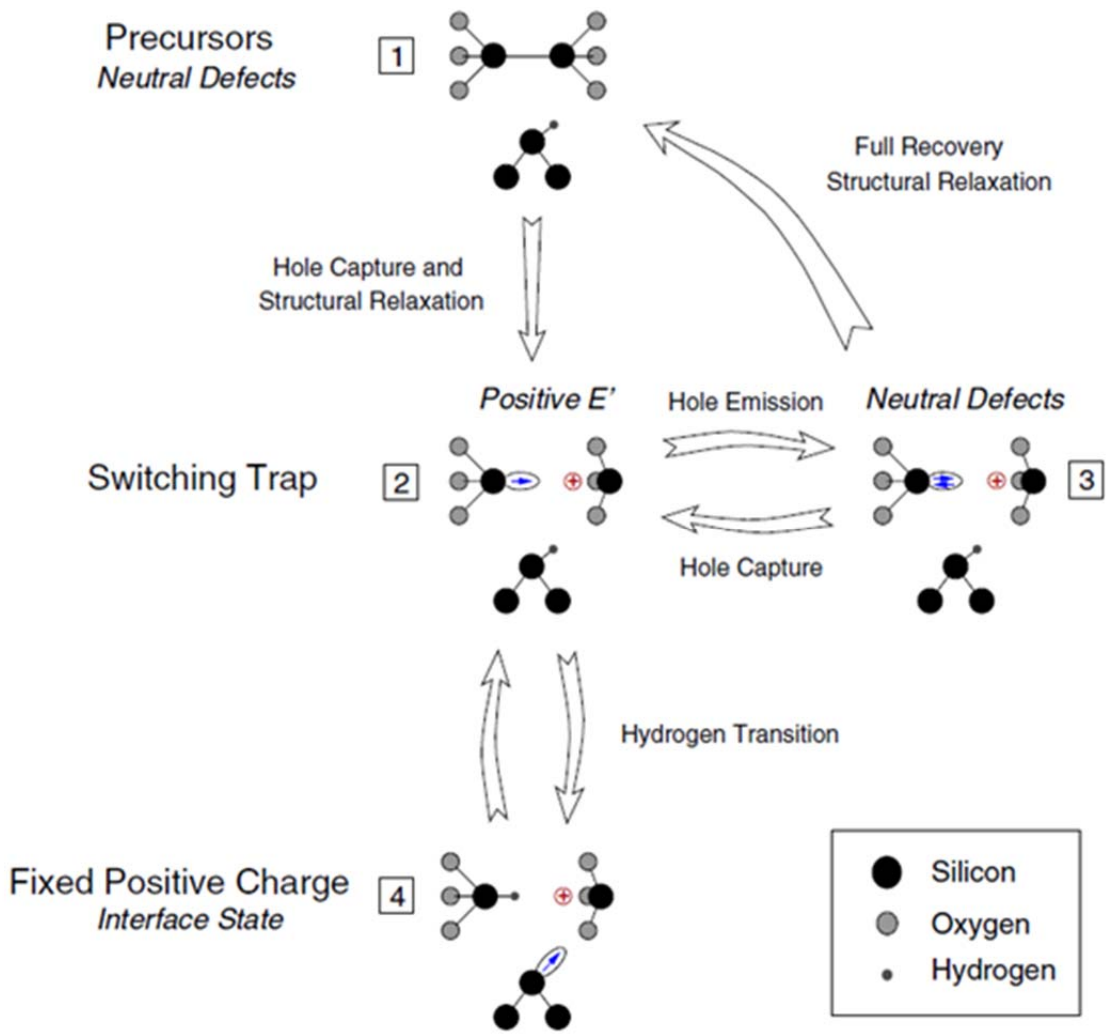

Figure 22. Switching traps process between E′- and P_b-centers, from [30].

In the discussion that follows, each of the state transitions in Figure 22 are described in detail—beginning with the precursor neutral defect state.

In State (1) neutral precursor defects known as E′-centers (Si—Si bond where each Si atom is back-bonded to three oxygen atoms) near the interface and P_b-centers (Si—H bond) at the interface are present in the material system as illustrated in Figure 23. The band diagram illustrates the location of the neutral E′-center precursor that resides is approximately 1 eV below the silicon valence band edge.

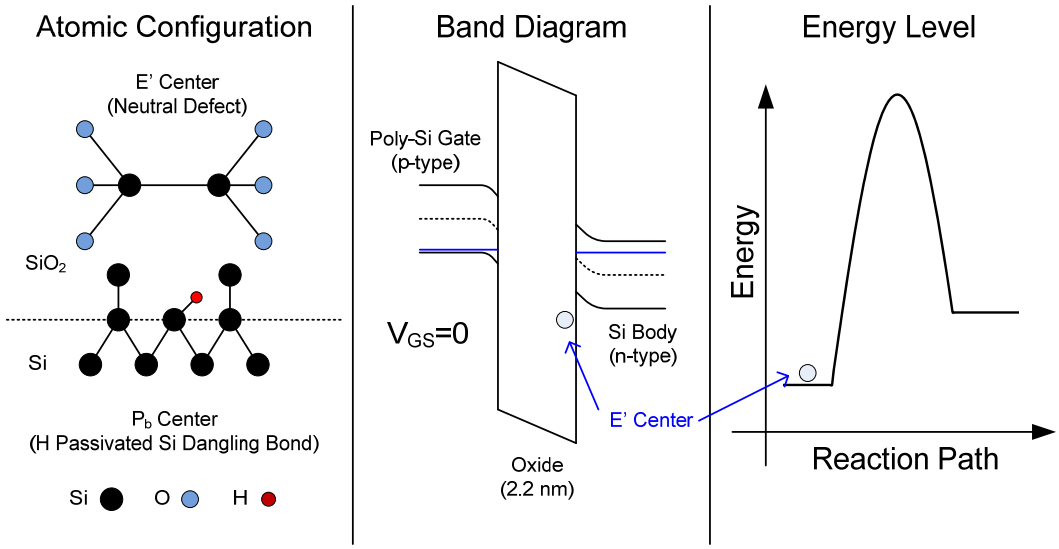

Figure 23. State (1), system prior to NBTI stress.

Once the NBTI stresses are applied, a lowering of the energy barrier occurs as a result of the applied electric field. Furthermore, holes accumulate at the interface as demonstrated in Figure 24.

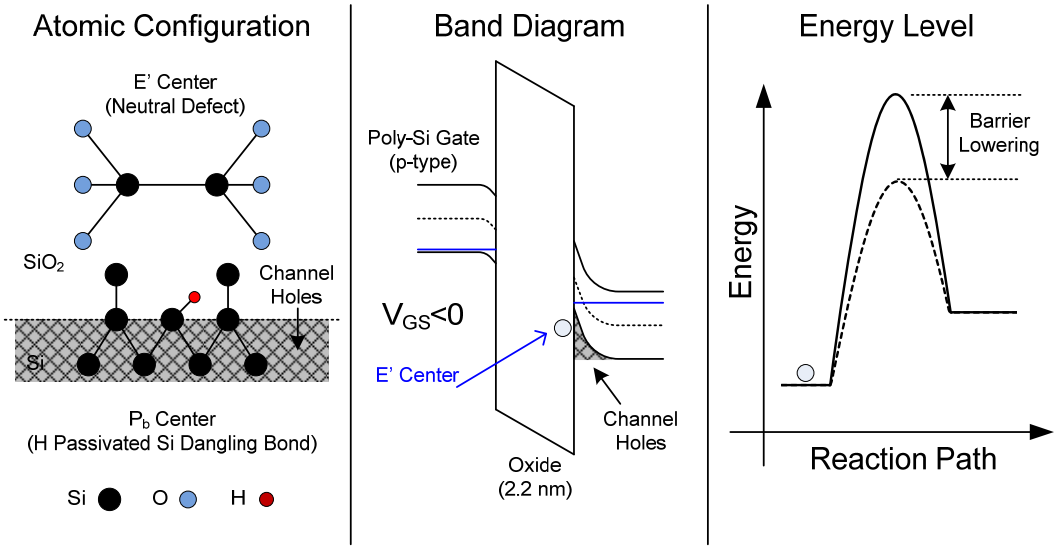

Figure 24. State (1), system under NBTI stress.

In Figure 25 a channel hole tunnels into the oxide in the vicinity of the E′-center precursor.

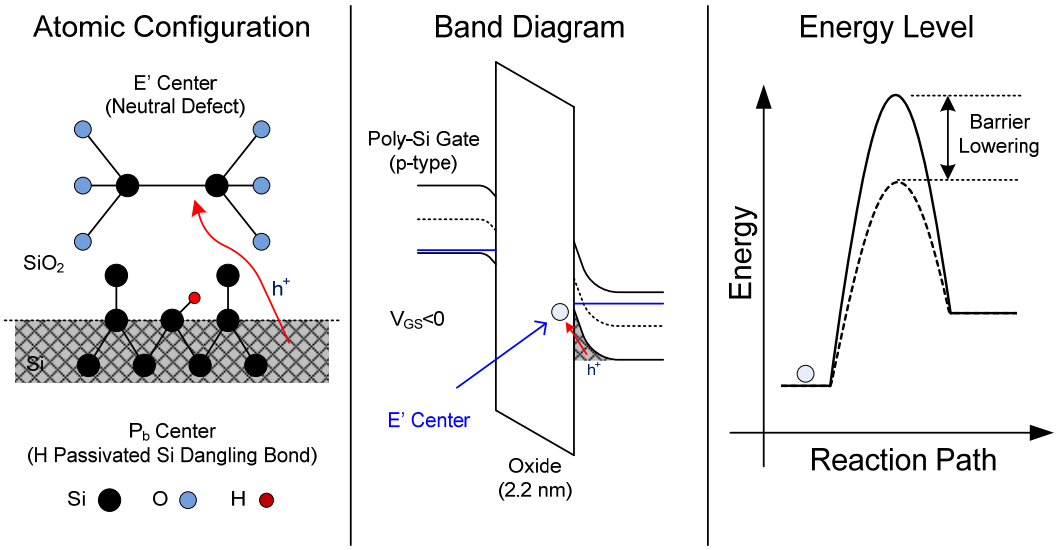

Figure 25. State (1) prior to hole capture and structural relaxation of the E′-center.

In Figure 26 the transition from State (1) to State (2) occurs when the hole becomes trapped resulting positive oxide charge followed by a structural relaxation on one Si atom and an unpaired electron on the other. The energy level of the activated E′-center increases as a result, residing in the lower half of the Si bandgap [31].

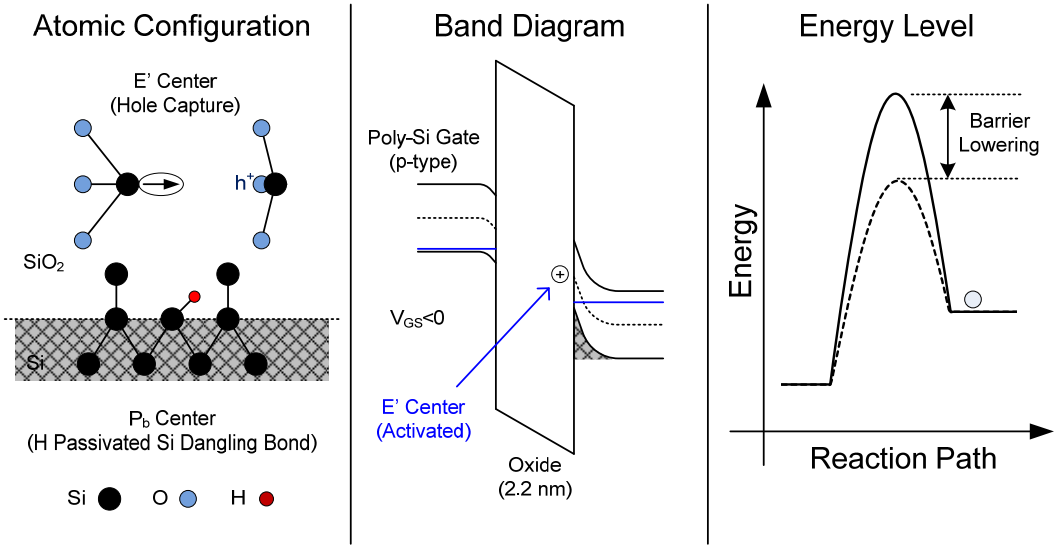

Figure 26. State (2), hole capture and E′-center structural relaxation.

In going from State (2) to State (4) the activation of the P_b-center occurs, by hydrogen dissociating from the interface, which in turn creates an interface state; this is followed by the H bonding with the unpaired Si electron thus becoming trapped as illustrated in Figures 27 and 28.

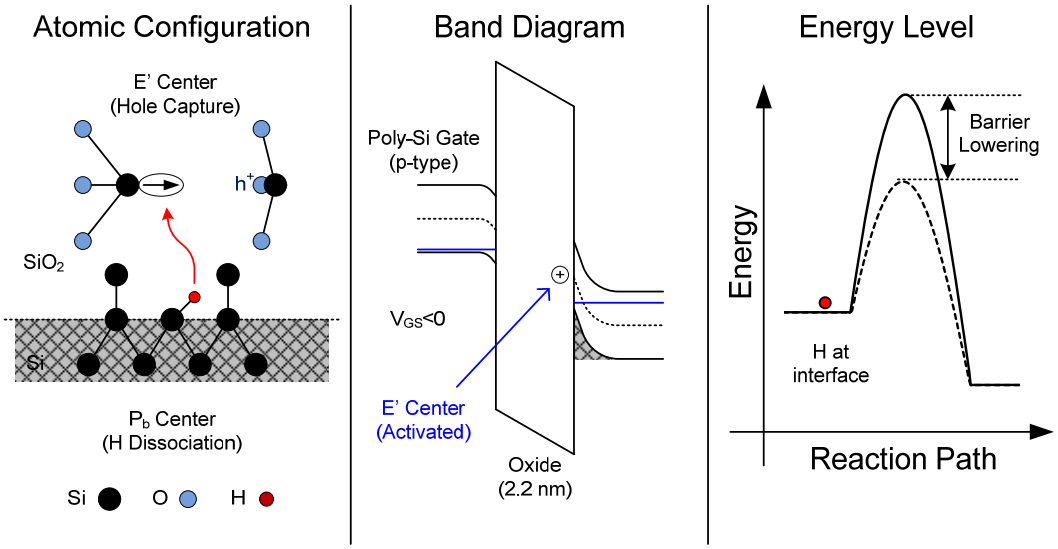

Figure 27. State (2) prior to H dissociation and interface trap generation.

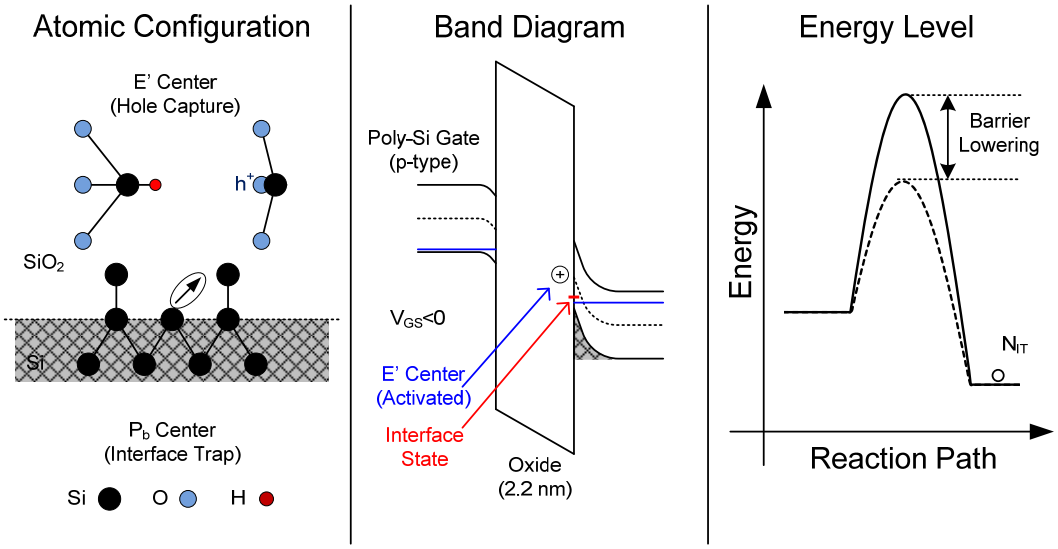

Figure 28. State (4) H capture at E′-center and interface state creation.

In going from State (2) to State (3) hole emission (electron capture) occurs neutralizing the E′-center defect (charge neutral). In this state, the energy level remains the same as the hole-trap state. From this state, it is possible for full recovery to occur retuning to State (1).

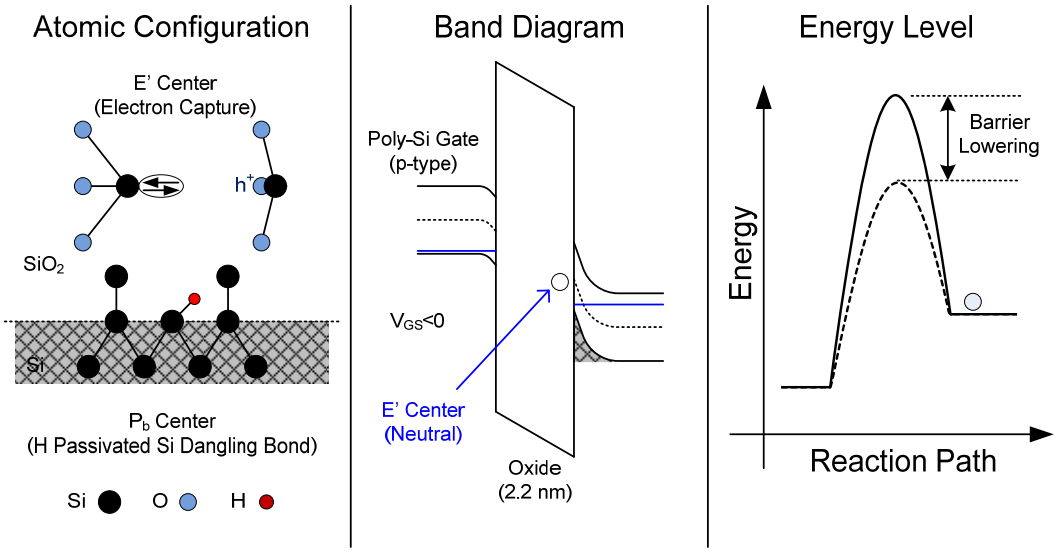

Figure 29. State (3), electron capture and E′-center neutralization.

For devices with oxides consisting of SiON, it has been shown by Lenahan et al. that K-centers (nitrogen vacancies) in the oxide function as P_b-centers did at the interface for SiO_2, calling the role of hydrogen in the process into question [15].

4. Characteristic (Empirical) Model for ΔV_T due to NBTI

Recall the equation for V_T degradation due to NBTI given by

$$\frac{\Delta V_T(t)}{V_{T0}} = A(E_{ox}, T)\ t^n, \tag{2.23}$$

where n is the power-law exponent and $A(E_{ox}, T)$ is a function of the vertical electric-field across the oxide and stress temperature. The $A(E_{ox}, T)$ term can be written as [12]

$$A(E_{ox}, T) = C_0\ f_E(E_{ox})\ f_T(T). \tag{2.24}$$

The coefficient C_o is a function related to the *Si—H* bond concentration at the interface and the exponential functions f_E and f_T are given by

$$f_E(E_{ox}) = E_{ox}^m \tag{2.25}$$

and

$$f_T(T) = e^{\frac{-E_A}{k_B T}}. \tag{2.26}$$

The equation for f_E is power-law dependent with exponent m on the applied electric field, E_{ox}. For f_T, E_A is the NBTI defect activation energy, and k_B is Boltzmann's constant. E_A and m are empirically obtained through device characterization under varying bias and temperature stress conditions. The field-dependent equation f_E need not be a power-law equation, but rather could be an exponential expression [32]. The exponential model for f_E would take the form

$$f_E(E_{OX}) = e^{\alpha E_{OX}} \tag{2.27}$$

The field-dependent degradation factor is given by the coefficient a in units of cm/MV.

The usefulness of Equation (2.23) is that it can be used (rewritten) to determine, the time-to-failure (TTF) of a device under a particular NBTI condition by invoking a boundary condition; for example, this can be accomplished by establishing a degradation criteria of $\Delta V_T/V_{T0} = 10\%$ and then solving for t to obtain the TTF

$$TTF = \left[\frac{1}{A(E_{ox}, T)} \left(\frac{\Delta V_T}{V_{T0}} \right)_{10\%} \right]^{1/n}. \tag{2.28}$$

A similar technique can be employed to characterize and predict TTF for other device parameters such as g_m, μ_{eff}, and I_{DS}.

5. Measurement Techniques for Characterizing NBTI

There are three main measurement techniques used to characterize NBTI: The stress-measure-stress (SMS), the on-the-fly (OTF), and the charge-pumping (CP) techniques. Each technique is utilized to capture specific information about the nature of the NBTI during stress and relaxation periods. The following gives a brief discussion of each technique.

a. Stress-Measure-Stress

The SMS technique is the conventional method for extracting ΔV_T. It does so by applying a negative bias stress at an elevated temperature for a period of time then temporarily removing the stress for device characterization as illustrated in Figure 30. Immediately after the characterization is completed, the stress is reapplied until the next measurement period is due.

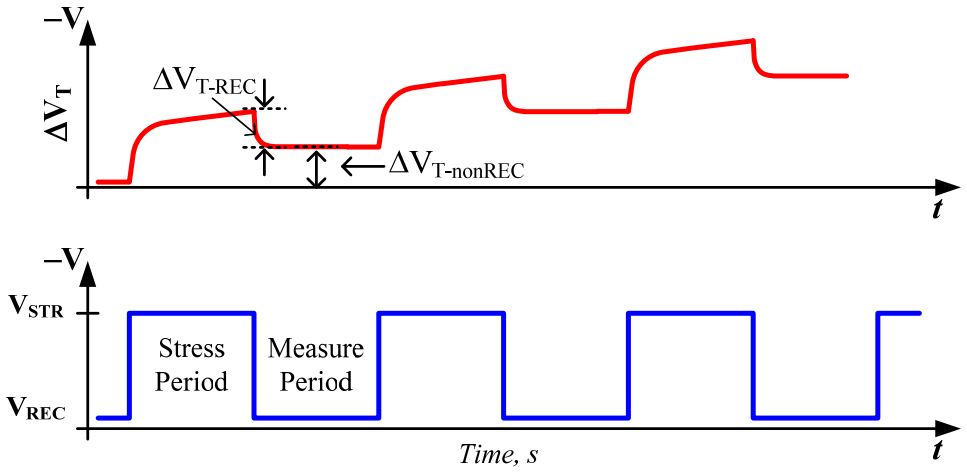

Figure 30. Illustration of the SMS method of ΔV_T extraction.

This technique is useful in determining the long-term V_T degradation. However, care must be used in its implementation as the instantaneous recovery component of NBTI may corrupt the long-term data if insufficient time elapses between stress removal and the start of the measurement phase. This technique was implemented in the device testing carried out in this research as described in detail in Chapter III.

b. On-the-Fly

The OTF techniques monitor the changes in I_{DS} in the linear region of operation in real-time; then, post-processing of the data converts the changes in I_{DS} to changes in V_T assuming that changes in I_{DS} are highly correlated to changes in V_T, and

$$\frac{\Delta i_{DS}}{i_{DS0}} \approx \frac{\Delta V_T}{V_{T0}}. \tag{2.29}$$

The usefulness of the OTF technique is that by monitoring changes real-time under stress conditions the real, or operational, V_T is extracted—inclusive of the fast recovery component. One of the drawbacks of the OTF methods is that a drain current must be flowing across the channel continuously—which means that the gate-voltage across the oxide is not uniform from source-to-drain; furthermore, if care is not taken in selecting the bias conditions, hot-carrier action may corrupt the data.

c. Charge-Pumping

The CP technique is primarily used to differentiate between the interface and oxide charge contributions to ΔV_T. It does this by flooding charge carriers into and out of the gate channel by applying voltage pulses to the gate. While the channel is in inversion, positive traps fill the energy gap; and, when the channel is in strong accumulation, the traps vacate. This trap charging and discharging at the interface is picked up electrically as a charge-pumping induced substrate current, i_{CP}. The interface trap density N_{it} can be extracted from the relationship [32]

$$N_{it} = \frac{i_{CP}}{q\ A_{ox} f_{CP}}, \tag{2.30}$$

where A_{ox} is the device gate area and f_{CP} is the frequency of the voltage pulses applied to the gate.

This technique is particularly useful because it allows the N_{it} extraction of minimum geometry transistors; however, this technique is difficult to implement as it is sensitive to bias during implementation which can introduce error is extracting interface traps. Furthermore, its usefulness on devices with ultrathin oxides is diminished due to tunneling currents overwhelming the i_{CP} component of the measurement.

D. IONIZING RADIATION: TOTAL IONIZING DOSE EFFECTS

1. Introduction

In the discussion that follows, charge trapping in the oxide and interface regions of the CMOS device as a result of total ionizing dose radiation is presented.

2. Ionizing Radiation Effects on MOSFET Devices

Ionizing radiation and TID effects cause charge trapping in the gate dielectric and isolating oxide regions of the MOSFET device and charge trapping in the field oxide regions between devices as demonstrated in the energy band diagram of Figure 31. When energetic particles encounter these regions of the semiconductor electron-hole pairs are created; and, under the influence of an electric field, the electrons being highly mobile compared to holes get swept up in the electric field and drift away leaving the less mobile positively charged hole behind in the oxide. Furthermore, interface states are created the Si-SiO_2 interface. The positively trapped charge and interface state creation results in a shift in the PMOS threshold voltage.

a. Electron-Hole Creation, Transport and Trapping

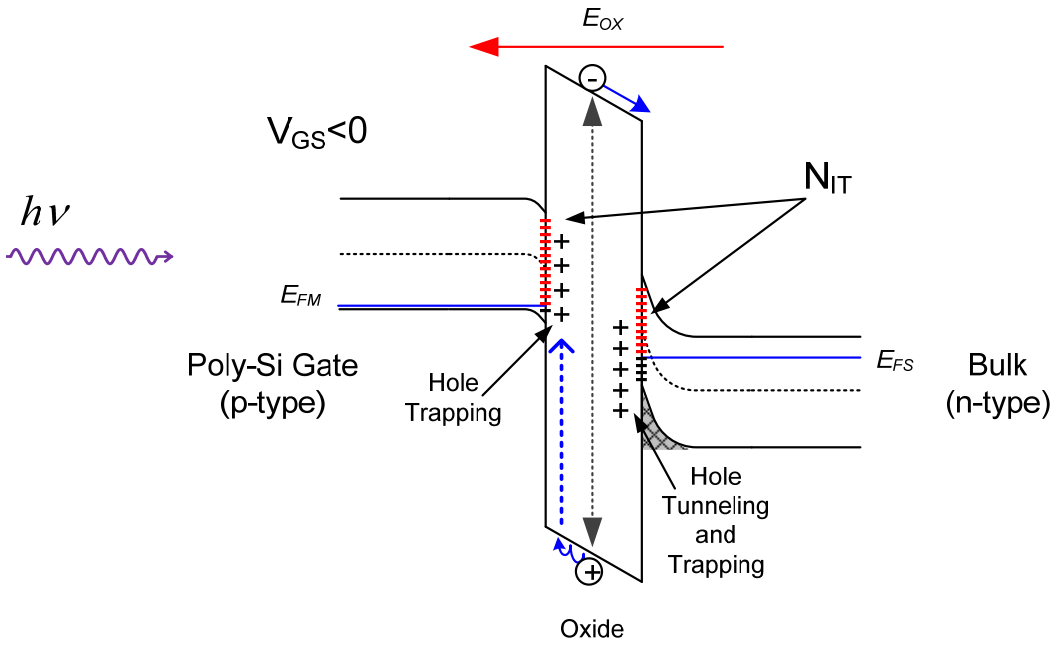

Figure 31. The effect of ionizing radiation on the PMOS device.

The ionizing process due to the radiation encountered by the PMOS device (SiO_2 on n-type substrate) is illustrated in Figure 31. The scenario unfolds as follows: a particle with kinetic energy $h\nu$, in which h is Planck's constant and ν is the particles frequency, encounters and reacts with the atomic structure of the gate oxide.

What occurs next is highly dependent on the particle energy, the material properties (bandgap energy E_G and work function, Φ) of the MOS structure and the electric fields present within the MOS device [33], [34]. However, assuming that the incident particle has energy sufficiently in excess of the SiO_2 bandgap ($h\nu \approx 18$ eV) [35] and that an electric field present in the oxide is on the order of magnitude of that encountered under normal operating conditions ($E_{ox} > 0.5$ MV/cm), the process is as follows:

- An electron-hole pair is generated due to the particle colliding with and losing energy to a valence band electron in the SiO_2.
- Given that the energy imparted on the valence band electron is in excess of E_G, the electron is excited into the conduction band leaving a hole behind.
- The electron, being highly mobile, gets swept across the oxide to the gate electrode by the electric field; and, the hole, being far less mobile than the electron, "hops" from localized state to localized state through the oxide toward the gate where it can become trapped at a deep hole trapping E′-center or tunnel out of the oxide into the poly-silicon gate.
- The abundance of holes at the Si-SiO_2 interface due to, and under the influence, of the electric field can tunnel into the oxide where they can become trapped at E′-centers.
- During the hole-transport process near the interface it is believed that the reaction of the hole with the E′-center allows for interfacial hydrogen bound to Si dangling bonds to dissociate from the interface P_b-center forming an interface trap N_{IT}.

To summarize, MOS devices, under favorable biasing conditions and exposed to ionizing radiation undergo *e-h* pair creation within the SiO_2 and the activation of precursor E′-centers to form positive oxide charge trap centers near the interface. Under the influence of E_{OX}, electrons are quickly swept out of the oxide; however, holes, having a much lower mobility in SiO_2 than electrons hop via localized states until they are captured at deep level traps near the SiO_2-gate interface. During the hole transport process, hydrogen dissociates from the interface, leading to the formation of interface traps. The ionizing radiation process thus results in three radiation-induced charge transport possibilities: oxide traps, E′-center hole traps, and interface traps (P_b precursor).

In Figure 32, the NBTI switching trap model described in detail in the previous section is presented here in its original form as proposed by Lelis et al. used to describe the charge transfer dynamics in SiO_2 due to ionizing radiation.

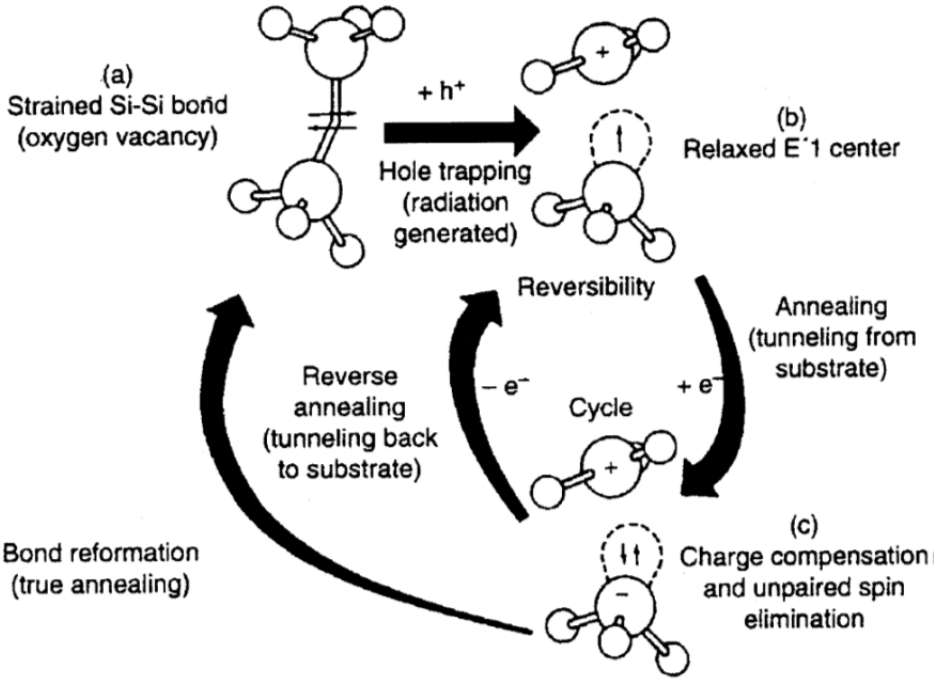

Figure 32. The HDL switching oxide trap model, from [28].

Where field and temperature stresses provided the energy to activate the E′-center in the switched trap model for NBTI, here ionizing radiation provides that energy.

However, at the time Lelis published his work, the role of interface traps with respect to hole trapping in this physical process was not well understood. As will be revealed later, the effect of ionizing radiation on the MOS device is highly dependent on biasing and temperature conditions.

b. Ionizing Radiation Effects on MOSFET Parameters

Oxide traps primarily affect the V_T of the MOS device due to the addition of positive oxide charge. Interface traps primarily affect the MOSFET effective mobility

but also have an effect on the V_T. The change in the V_T manifests itself as a change in the device V_{FB}:

$$\Delta V_{FB} = -\frac{\Delta Q_{OT}}{C_{ox}} - \frac{\Delta Q_{IT}(\phi_S)}{C_{ox}}. \tag{2.31}$$

It is important to note that Q_{OT}, as was the case for Q_M, is a function of the centroid of the charge distributed throughout the oxide relative to the metal-oxide and oxide-semiconductor interfaces. The closer the centroid to the oxide-semiconductor interface, the stronger the influence the trapped charge has on the V_{FB}.

The ΔQ_{IT} due to the change in N_{IT} will manifest as degradation in not only the change in V_T due to ΔV_{FB}, but also in the effective channel mobility. From the work of Sexton and Schwank [36] it was demonstrated that the mobility degradation could be fitted to an analogous empirical model given by

$$\mu_{eff} = \frac{\mu_o}{1 + \alpha(\Delta N_{it})}. \tag{2.32}$$

For the NMOS device, the oxide traps have a decreasing effect on the device V_T whereas the interface traps being negative in nature for the n-channel device have the effect of increasing the threshold voltage. For the PMOS device, both interface traps, being positive in nature for p-channel devices, and positive oxide charge both work to decrease (increase in magnitude) PMOS V_T. In terms of device performance, generally the NMOS transistor becomes harder to turn off and the PMOS transistor harder to turn on due to V_T shifts due to oxide trapping. However, both also suffer from channel mobility degradation resulting in the degradation of g_m and the transistor drive-current I_{ON}, also known as the drain current in saturation I_{DSAT}, due to interface charge trapping.

The effects of oxide and interface trapping on the *I-V* characteristics are given in the plots of Figure 33 in which the curves demonstrate the effects of positive oxide traps and the spreading of slope of the post irradiated device indicative of interface traps.

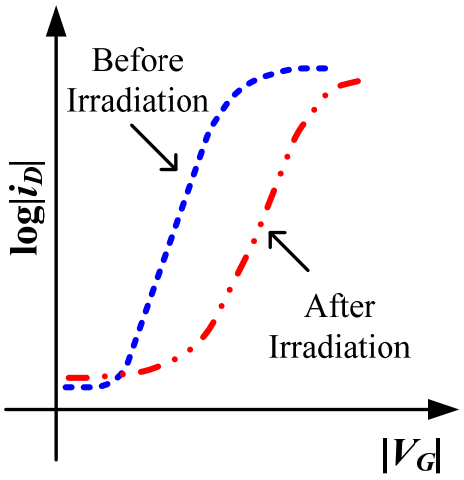

Figure 33. I_D-V_G curves demonstrating radiation effects on an PMOS device.

3. Ionizing Radiation Effects on Modern Devices

It is commonly accepted that TID effects in state-of-the-art semiconductor processes will be minimal [17]. This is due to the smaller gate-oxide thicknesses and cross-sectional areas (i.e., smaller gate area of the transistor) that are a result of the course of device scaling. This is supported by predictions made by Pierret [10] where it can be shown that ΔV_T due to oxide traps is proportional to the square of the oxide thickness t_{ox}. Due to these thinner oxides, it is also surmised that the increased gate leakage currents from electron tunneling in advanced technology nodes has a larger effect, to many orders of magnitude, than those as a result of ionizing radiation.

Though the trend of reduced total dose effects reported as a function of advancing technology node supports this assertion there have also been reports of enhanced TID effects due to the increase in the number interconnect layers inherent in state-of-the-art processes [18], [19]. Furthermore, high-k dielectrics, used to minimize gate tunneling currents by allowing thicker gate oxides to be manufactured while maintaining or improving the transistors drive strength, have larger gate-oxide volumes which could give rise to increased charge trapping in the gate oxide as a result of ionizing radiation as demonstrated in [20].

E. COMPARISON OF PHYSICAL MECHANISMS

As presented in the two previous sections, TID radiation and NBTI can affect the same PMOS device parameters (V_T, g_m, μ_{eff}, and I_D) with similar electrical degradation characteristics. While both degradation due to ionizing radiation and NBTI involve the activation of trap centers and the trapping of carriers at the interface and within the oxide, the processes by which the trap centers are activated are not similar. For NBTI, the activation of trap centers and charge trapping is achieved by an applied negative gate bias at an elevated temperature; whereas, for TID, the activation of trap centers and charge trapping are a result of energetic particles incident on the gate-oxide and adjacent bulk and gate-poly regions producing an excess of *e-h* pairs—possibly in the presence of an applied bias enhancing the process. However, it is believed that both NBTI and TID radiation activate and engage the same defect centers; E′-centers in the oxide and P_b-centers at the Si-SiO_2 interface (or, alternatively, K-centers in the case of nitrided oxides).

It has been frequently stated in the literature that NBTI in PMOS devices is the most pressing reliability concern of the day. At the same time, it has been suggested that due to decreased gate-oxide volumes resulting from ultra-thin dielectrics that oxide traps due to ionizing radiation should be minimal.

However, research reported in the literature on the combined effects of NBTI and TID radiation is minimal [17], [20], [21]. For older technologies, NBTI was not yet a substantial reliability threat; on the other hand, TID effects were. For newer technologies, NBTI is a pressing reliability issue; but TID effects are assumed not. However, with the introduction of new material systems with larger gate-oxide volumes and higher sensitivity to BTS, both TID radiation and NBTI effects could be an issue during the same era.

Research initially performed by Zhou [20] and continued by Chen [21] examined high-k capacitor structures manufactured in a research environment and concluded that, in the case of early high-k dielectric structures, the combined effects of BTS after ionizing irradiation was worse than the sum of the effects performed separately. Though the subsequent results reported by Chen on refined high-k devices showed improved

results, subsequent research on the combined effects of TID radiation and NBTI on devices produced on commercially available CMOS processes has not been reported in the literature.

In the research performed by Zhou experimental capacitors of HfO_2- Al_2O_3- and SiO_2-based dielectrics were formed on p-type, n-type and n-type Si substrates, respectively. The capacitors were exposed either to X-ray radiation, or BTS, or to X-ray radiation prior to BTS induced degradation. It was demonstrated for certain combinations of bias during irradiation and post-irradiation BTS conditions that the combined effects were much worse than the effects observed separately; with the worse case being devices irradiated under positive- or zero-gate bias then subjected to negative BTS. The results for the HfO_2-based devices under various cases of irradiation and stress bias conditions are summarized in Figure 34.

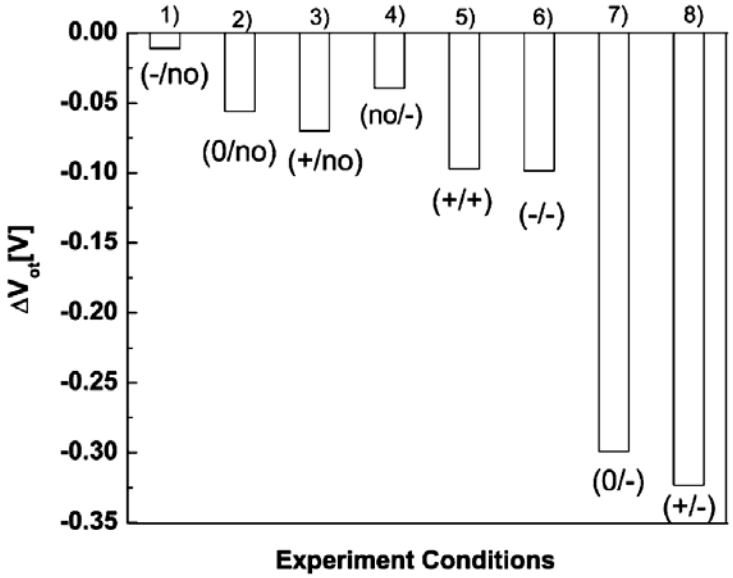

Figure 34. Experimental results of TID, BTS, and combined TID and BTS, from [20].

The conditions the devices were subjected to during experimentation are given within the parenthesis, "(#/#)," where the "-" indicates negative bias, the "+" positive bias, the "0" zero-bias, and "no" indicating the respective experiment was not performed. Of particular interest is the observation that the sum of the degradation seen in Case 2

(zero-bias TID, no BTS) and Case 4 (no TID, NBTI) is much-much less than the degradation seen in Case 7 (zero-bias TID followed by NBTI). A similar observation can be made with regards to Cases 3, 4, and 8. Clearly, for this material system, the BTS response is significantly enhanced by the TID. The authors attribute these results to the creation of oxide dipoles during irradiation after which, the dipole electrons are then swept from the oxide during BTS. The scenario for Case 7, a SiO_2-based PMOS device is illustrated in Figure 35.

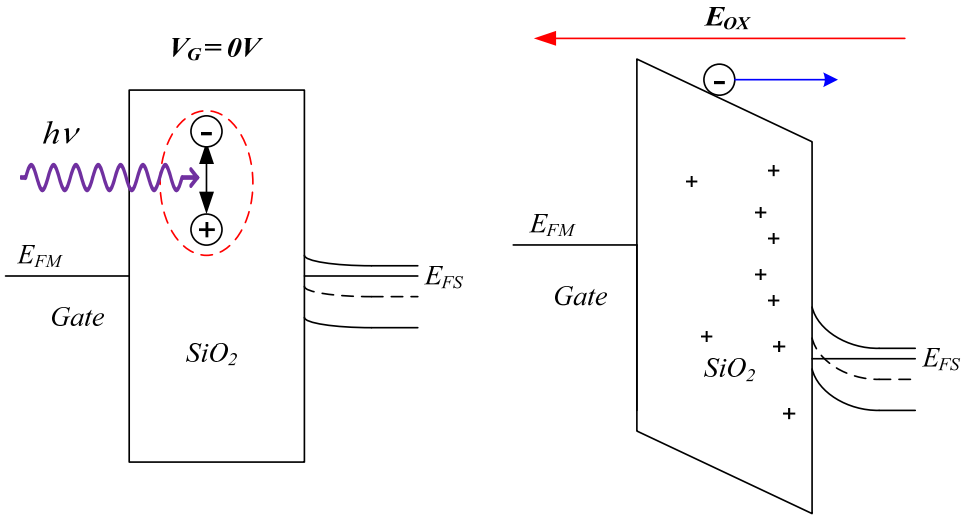

Figure 35. Case 7: Zero-bias irradiation (left) followed by NBTI (right).

The worst case for the Al_2O_3- and SiO_2-based devices was observed for negative bias during irradiation and NBTI. For the SiO_2-based device, the worst-case result coming under negative bias during irradiation is somewhat inexplicable as it appears to be, admittedly by the authors of the research and without explanation, generally at odds with the literature. Based on their results, the authors propose that for a SiO_2-based p-channel MOS capacitor, the worst case response for the device would be for it to be subjected to a negative bias during irradiation, followed by NBTI.

However, it is this author's opinion that based on the literature, research, and analysis presented in this chapter that a potential worst case, and operationally relevant, scenario for PMOS devices will be radiation exposure under zero-bias condition followed

by NBTI. The kinetic nature of the degradation could be the creation of dipoles within the oxide during irradiation, specifically radiation induced activation of precursor E′- or K-centers, followed by hole-capture and structural relaxation during NBTI, leading to an enhancement of NBTI process and its effects on device parameters.

F. CHAPTER CONCLUSION

This chapter began with the introduction of the PMOS material system under study and a discussion of the MOSFET threshold voltage. This was then followed by a discussion on the background, characteristics, and controversy surrounding NBTI in PMOS devices—this unfolding story is still unresolved. This discussion then led us into the subject of TID radiation effects in these same devices. Finally, the realization that very possibly the same defect centers (E′- and P_b-precursors) and physical mechanisms (trap-switching) within the MOS device are common to TID radiation and NBTI in PMOS devices. In the chapter to follow, the experimental approach for evaluating this realization is explored.

III. EXPERIMENTAL APPROACH FOR EVALUATING THE COMBINED EFFECTS ON THE P-CHANNEL MOSFET

The discussion of Chapter II concluded with the combined effects of irradiation and bias-temperature stress which, through the work of Zhou, demonstrated that the combined effects of irradiation and bias temperature stress can be far worse than the sum of the effects taken separately [20]. This potential for accelerated degradation leads to the question: how do the results of Zhou, obtained from experimental capacitors introducing novel material systems, compare to the material system being researched in this dissertation?

Toward answering this important question, the overarching experimental methodology employed in the device characterization is given, followed by the description of the apparatus used in the carrying out the methodology. Finally, the chapter concludes with the determination of the electrical and environmental parameters needed to demonstrate and evaluate the sensitivity of this material system to TID radiation and NBTI.

A. COMBINED EFFECTS—EXPERIMENTAL APPROACH

In this section, the experimental approach toward investigating the combined effects of TID radiation and NBTI on the p-channel MOSFET is presented. With MIL-STD-883H, Method 1019.8, "Ionizing Radiation (Total Dose) Test Procedures" and the JEDEC Standard, JESD90, "A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities" as references, the discussion begins with the experimental methods employed; followed by the test and measurement apparatus used in the experiments. Details are then given describing the preparation of the devices for the experiments.

1. Experimental Methods

In this section, the two experimental methods used as frameworks in carrying out the experimental approaches are presented. First, the method for performing the ionizing radiation followed by NBTI experiments is discussed which is then followed by a

discussion of the method used for completing the concurrent ionizing radiation and NBTI experiments.

a. TID Irradiation Followed by NBTI

In Figure 36, the test flow diagram prescribed by Method 1019.8 was adapted to include the JESD90 standard for the purpose of carrying out NBTI characterization following TID irradiation on the devices under test.

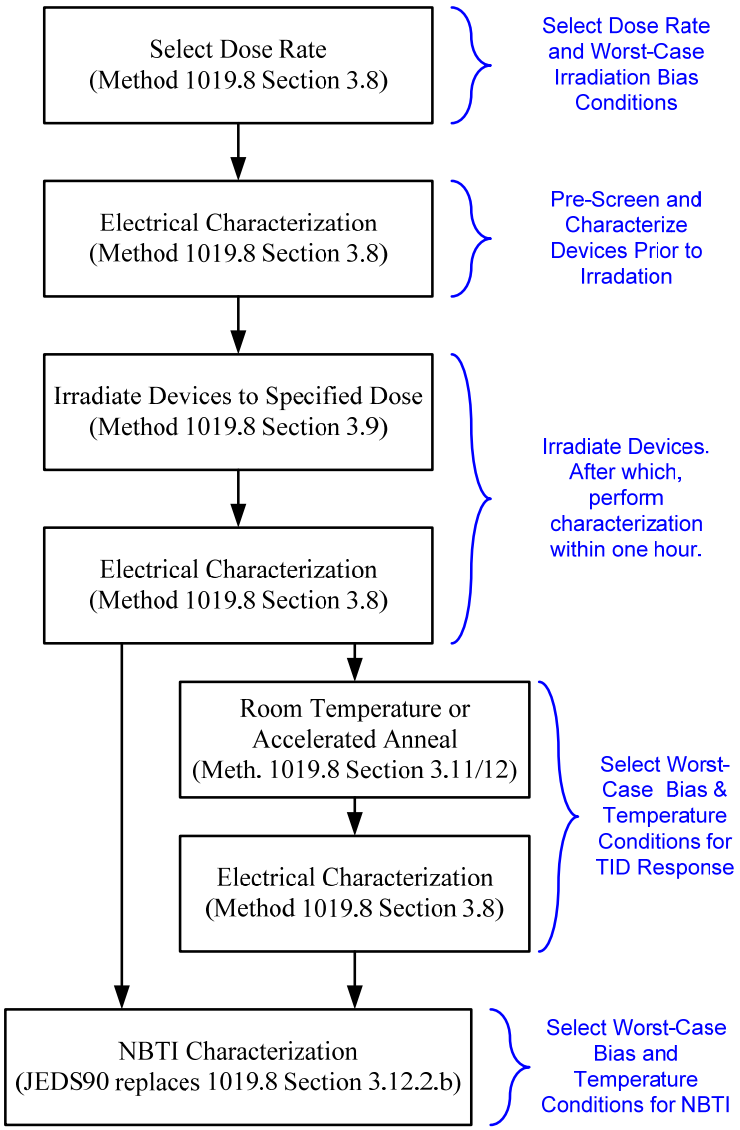

Figure 36. Modified Method 1019.8 (MIL-STD-883H) flow for NBTI after TID.

In essence, Section 3.12.2.b of Method 1019.8 which calls for the accelerated annealing of the test device by subjecting the device to worst-case static bias conditions at an elevated temperature after irradiation was replaced with JESD90 which calls for NBTI testing with bias and temperature conditions favorable for characterizing device NBTI. Since the purpose of the experiments was to characterize the devices, pass/fail criteria normally part of the prescribed flow were not applicable. The adapted flowchart also shows an option to carry out a room temperature or accelerated anneal after TID irradiation prior to NBTI.

The stress-measure-stress flow for carrying out the NBTI characterization in Figure 36 is detailed in the test flow diagram of Figure 37. Under this flow, device stressing is performed with a constant-voltage bias applied to the gate terminal at an elevated temperature. The voltage stress is periodically removed to perform device characterization; after which, the stress is reapplied for the next cycle until all stress cycles are completed. It is standard under JESD90 for the stress interval to take on a logarithmic progression (i.e., 1, 3, 7, 10, 30, 70, … 700,000 seconds) due to logarithmic nature of the ΔV_T degradation; however, data may need to be collected on a shorter time interval.

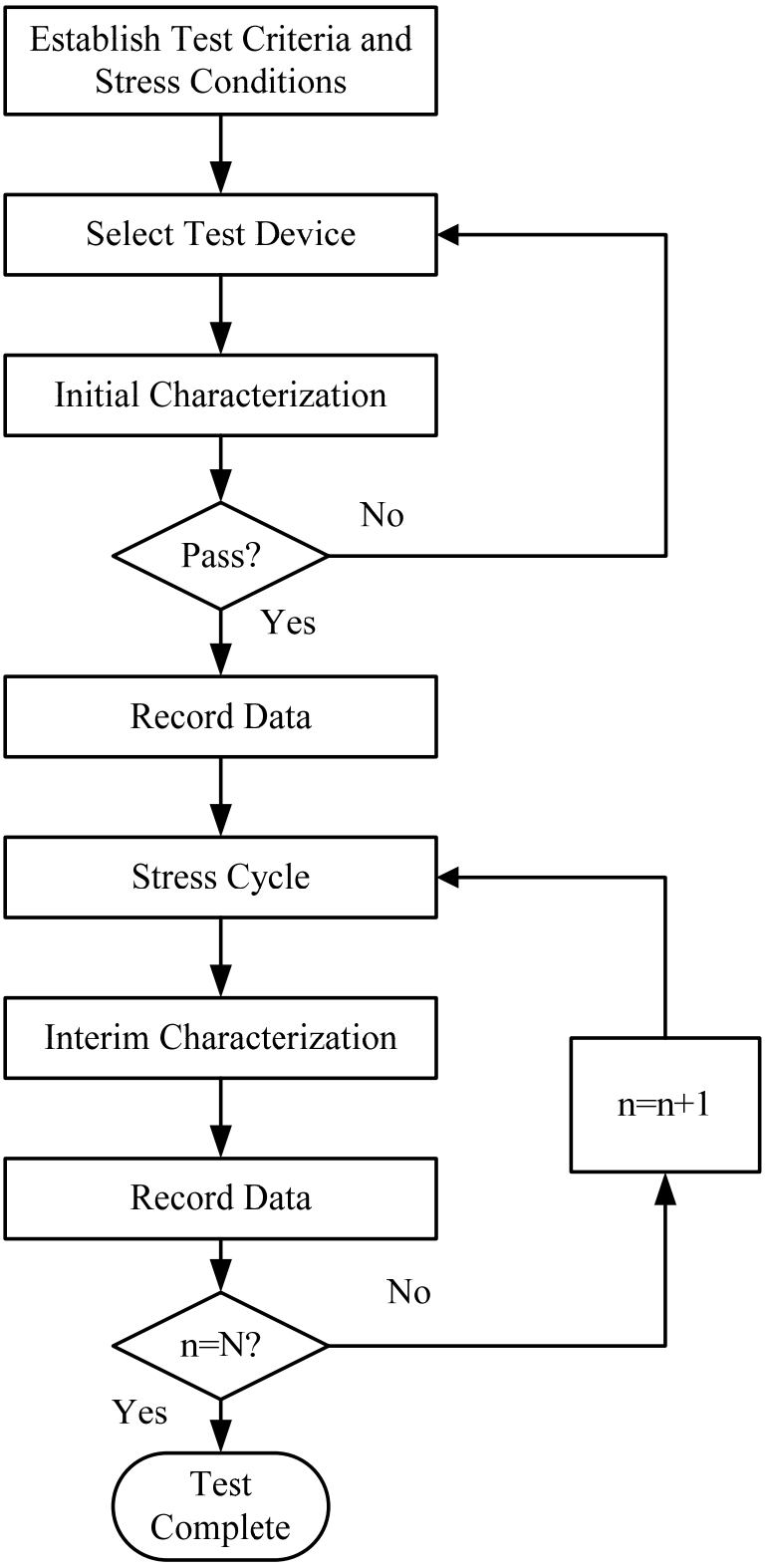

Figure 37. NBTI Characterization test flow.

b. Concurrent TID Radiation and NBTI

The flowchart of Figure 37 provides an equally applicable methodology for carrying out NBTI characterization while the device is being irradiated. In this regard, ionizing radiation was incorporated into the NBTI test and TID treated as an additional environmental variable. The experiments carried out under this methodology were designed to investigate the progression of NBTI in an ionizing environment. As of this writing, there have been no reports in the literature of the characterization of NBTI while the device is being subjected to ionizing radiation.

2. Apparatus

The radiation source was a J. L. Shepherd and Associates Co-60 irradiator that produce 1.25 MeV gamma-rays, at the DoD's Defense MicroElectronics Activity (DMEA) Science and Engineering Gamma Irradiator Test (SEGIT) facility located in McClellan, CA. For irradiations and concurrent NBTI testing at elevated temperatures, a Dewar temperature system (DTS) environmental chamber was incorporated with the irradiator. The DTS system is capable of temperature control over the range of -150 to 150 degrees Celsius. A Tenney environmental oven was used for elevated temperature testing of devices post-irradiation. Bias stressing was achieved with the use of a HP-6626A 4-channel power supply. The bias stress control, test program, and data collection were accomplished via a Keithley semiconductor characterization system consisting of the Keithley 4200-SCS parameter analyzer and integrated Keithley 707A switch matrix. Experiments of packaged devices involving the DTS or Tenney environmental oven utilized an interface printed circuit board and cabling system between the 707A switch matrix and the device under test (DUT) board.

The block diagram of Figure 38 represents the configuration for experiments involving radiation followed by NBTI; and, the block diagram of Figure 39 represents the configuration used for devices subjected to ionizing radiation during NBTI.

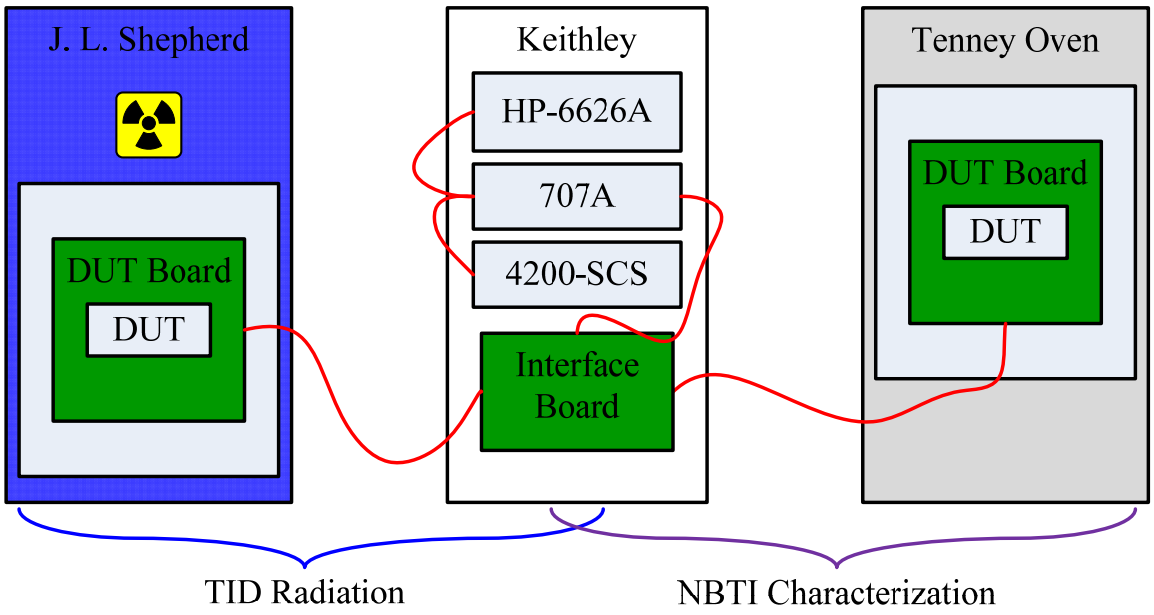

Figure 38. Apparatus configuration for TID (left) and NBTI (right).

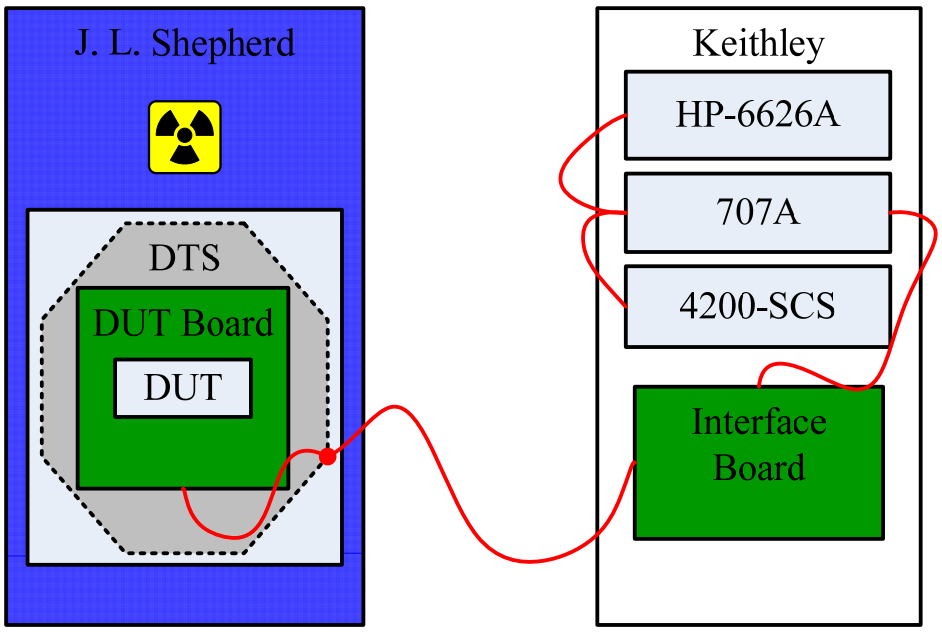

Figure 39. Irradiator with the DTS integrated for TID while NBTI.

MATLAB was used extensively in the post-processing of the raw experimental data collected by the Keithley system.

3. Device Preparation

Devices under test were either packaged in an 18-pin ceramic dual in-line package (cerDIP), probed at the wafer level, or die mounted on a substrate for probing. Wafer saw, die packaging and mounting took place primarily at the DMEA packaging and assembly facility.

B. DETERMINATION OF THE EXPERIMENTAL CONDITIONS

This section discusses the establishment of the experimental conditions necessary to characterize the NBTI response following, or during, exposure to ionizing radiation. Since the reported device responses to ionizing radiation and NBTI varies greatly in the literature due to the differences in material systems and experimental factors such as bias, temperature, and annealing, an approach was established to identify those conditions during irradiation and post-irradiation anneal that would produce an exacerbated NBTI response in devices subjected to post-irradiation and anneal NBTI.

However, before one can study the effects of ionizing radiation on the NBTI response, an understanding of the device pre-irradiation NBTI characteristics is needed. In what follows, the experimental conditions for characterizing device NBTI is presented, followed by the experimental conditions required during irradiation and anneal to identify those conditions with the potential of exacerbating the NBTI response.

The organization of the three experiment groupings for which bias and temperature conditions are established in this dissertation toward investigating the effects of ionizing radiation on NBTI are shown in Figure 40.

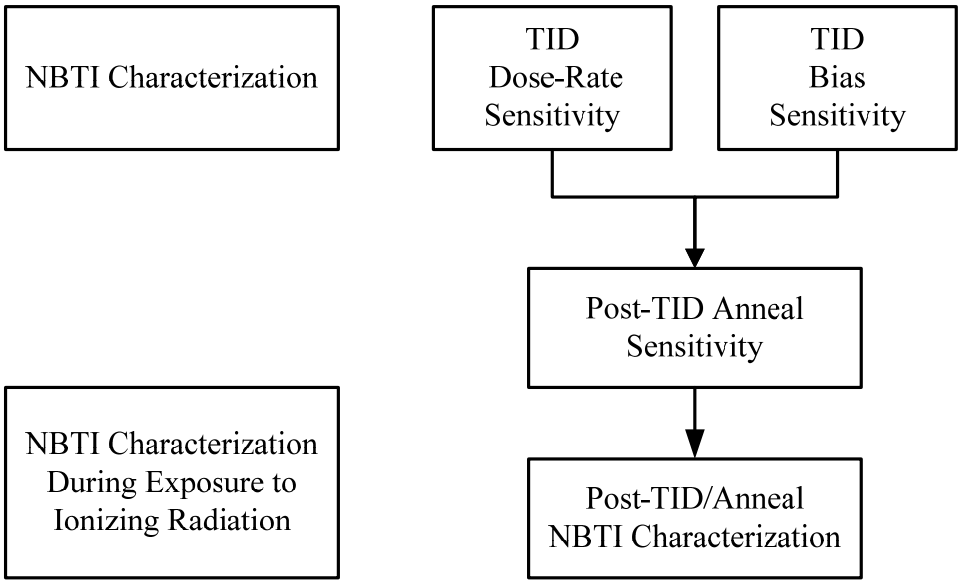

Figure 40. Experiment groupings: NBTI; TID-Anneal-NBTI; and, NBTI while TID.

1. Experimental Conditions for NBTI Characterization

For the p-channel MOSFETs of this research, a process model consistent with that used in the semiconductor industry [12], [32] for the ΔV_T due to NBTI was provided by the foundry and is given by

$$\Delta V_T = \frac{500 \times Z}{500 + Z} \tag{3.1}$$

where

$$Z = A_0 \times e^{\frac{-\Delta H}{kT}} \times \left(\frac{|V_G|}{T_{ox}} \right)^m \times t^n \times |V_{T0}|^l \times \left[1 + \left(\frac{a_W}{W_D} \right) \right]. \tag{3.2}$$

The parameters for Equation (3.2) are given in Table 1. Due to non-disclosure considerations, the reported process parameter values have been omitted from the table. However, from Equations (3.1) and (3.2), and knowledge of the parameters given in Table 1, it is possible to establish the ΔV_T dependence on the applied E_{OX}, T, and stress duration t_{eq} for a given designed gate width W_D due to NBTI—prior to conducting any experiments.

Table 1. NBTI ΔV_T equation parameters

Parameter	Description	Units
ΔV_T	Shift in threshold voltage	mV
ΔH	Activation energy	eV
T_{ox}	Gate oxide thickness	nm
V_G	Gate voltage in volts	V
t_{eq}	Equivalent dc stress time in seconds	s
a_w	Width dependence	μm
W_D	Device design width	μm
T	Junction temperature	K
k	Boltzmann's constant (8.62×10^{-5})	eV/K
V_{T0}	Initial threshold voltage at T_{STR}.	V
A_0	Process dependent pre-factor coefficient	--
m	E_{OX}-dependent exponent	--
n	Time-dependent exponent	--
l	V_{T0}-dependent exponent	--

This was useful in two regards; first to establish a reasonable set of bias and temperature conditions from which to conduct the experiments and secondly to validate the experimental results obtained thereby establishing a baseline from which further experimentation could take place.

The minimum set of temperature and voltage combinations needed for establishing NBTI dependence on E_{OX} and T for the devices being researched are presented in Table 2.

Table 2. Temperature and voltage parameters for characterizing NBTI.

T_{STR} / V_{STR}	85 C	100 C	125 C
−1.5 V			√
−1.9 V			√
−2.3 V	√	√	√

The voltage/temperature combinations were selected with the goal to promote a sizable ΔV_T response within a reasonable amount of time without inducing secondary degradation effects such as TDDB and HCI. Therefore, V_{STR} was selected to keep E_{OX} below the critical E-field of 10 MV/cm. The stress temperatures T_{STR} were selected based on the commonly accepted commercial (85 C), industrial (100 C), and military (125 C) maximum operating temperatures. Figure 41 demonstrates the ΔV_T based on the form of the process model equation for three selected voltage and temperature combinations, of Table 2. The plots of ΔV_T in Figure 42 demonstrate the dependence of ΔV_T on T_{STR} and V_{STR} and can be characterized by

$$\Delta V_T = B\left(T_{STR}, V_{STR}\right)t^n. \tag{3.3}$$

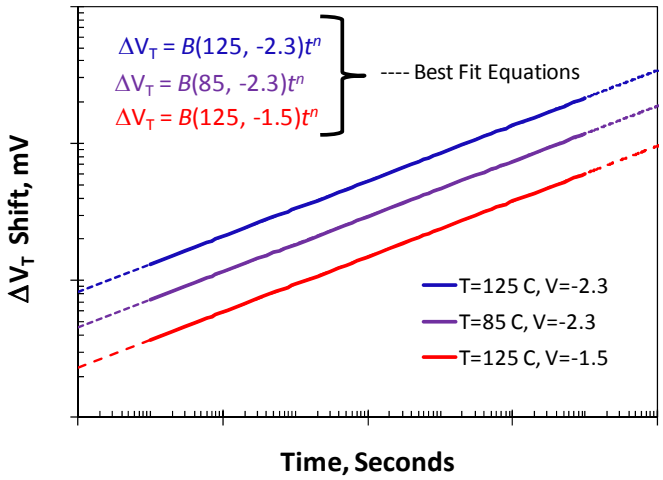

Figure 41. PMOS NBTI induced ΔV_T vs. *time* from Equation 3.1.

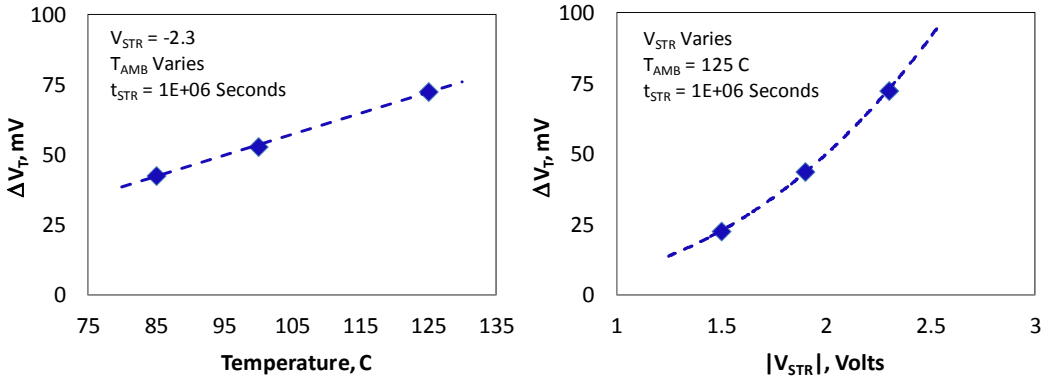

Figure 42. Plots of ΔV_T vs. T_{AMB} and V_{STR}, respectively.

2. Establishment of TID Experimental Parameters

Two sets of experiments were devised and parameters established to determine device NBTI sensitivity to ionizing radiation in which the first set explores the bias and anneal sensitivities while the second set explores the potential dose-rate sensitivities of NBTI. These are discussed next.

a. Bias and Anneal Experimental Parameters

The device response to TID under varying bias and temperature conditions during irradiation, anneal, and subsequent BTS varies greatly in the literature due to varying device processing techniques, material system composition, and device type. Without a basis for the material system under examination, it is important to go through the process of identifying and evaluating conditions that have the potential for bringing about unacceptable levels of device degradation. The diagram of Figure 43 outlines the test flow employed that follows the modified MIL-STD-883 Method 1019.8 and JESD90 presented previously in Figure 37. The experimental details are provided in Table 3.

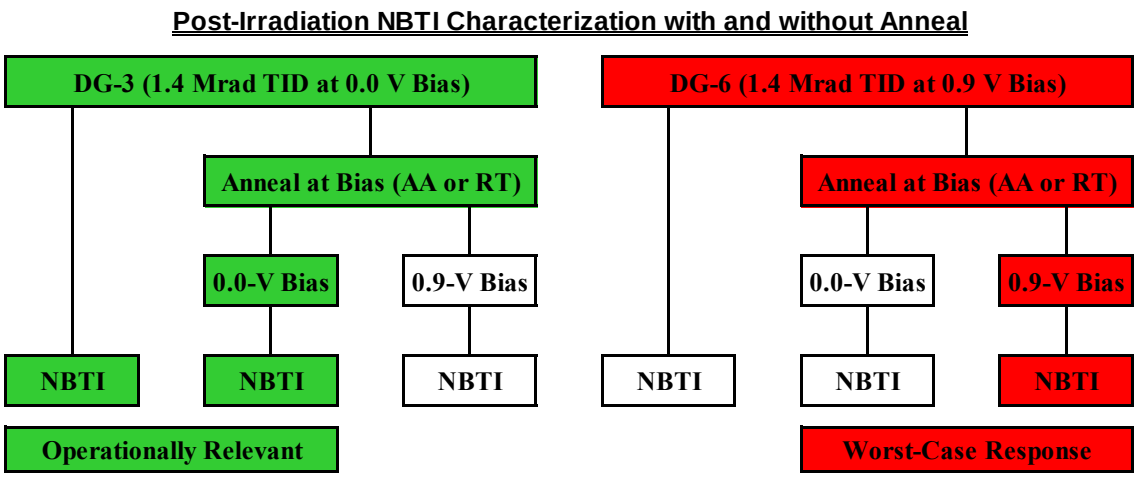

Figure 43. Experimental flow from TID to NBTI characterization.

Table 3. Detailed experimental parameters.

Radiation Exper. Cond. & TID Exposure (rad-SiO_2)							Anneal					NBTI Exper. Conditions			
V_{STR} (Volts)	E_{OX} (MV/cm)	T_{amb} (C)	*in situ* Char?	TID (Mrad)	Dur. (Hrs)	Dose Rate (Rad/sec)	V_{STR} (Volts)	E_{OX} (MV/cm)	T_{amb} (C)	*in situ* Char?	Dur. (Hrs)	V_{STR} (Volts)	E_{OX} (MV/cm)	T_{amb} (C)	Dur. (Hrs)
0.0	0.0	25	N	1.4	3	129.6	No Anneal					-2.3	7.2	125	24
0.0	0.0	25	N	1.4	3	129.6	0.0	0.0	25	N	168	-2.3	7.2	125	24
0.0	0.0	25	N	1.4	3	129.6	0.0	0.0	125	N	168	-2.3	7.2	125	24
0.0	0.0	25	N	1.4	3	129.6	No Anneal					-2.3	7.2	125	24
0.0	0.0	25	N	1.4	3	129.6	0.0	0.0	25	N	168	-2.3	7.2	125	24
0.0	0.0	25	N	1.4	3	129.6	0.0	0.0	125	N	168	-2.3	7.2	125	24

The irradiation bias, temperature, and anneal conditions were chosen to minimize BTI, HCI, and TDDB degradation mechanisms during the irradiation and anneal while demonstrating promise for an exacerbation of the NBTI response such as those demonstrated by Zhou [20] and Schwank et al. [37]. An example of this is presented in Figure 44 in which, post-anneal BTS instability was exhibited in devices (n-channel MOSFETs) known typically not to be susceptible to such phenomena.

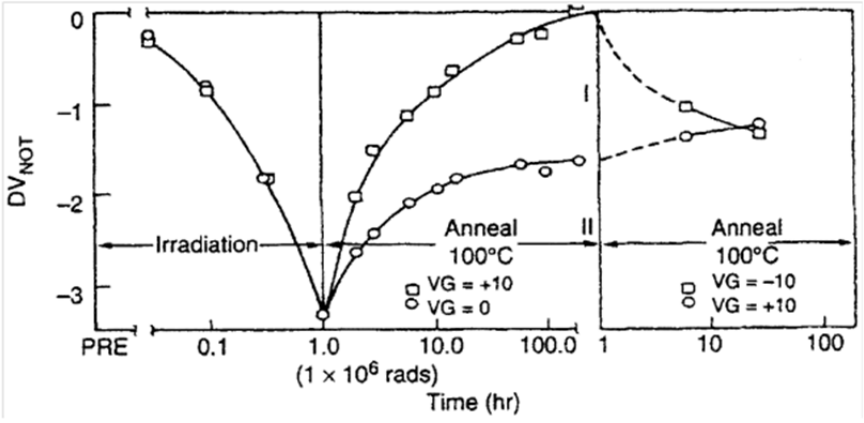

Figure 44. Device response to irradiation, anneal, and BTS, from [37].

Once experimental conditions favorable to eliciting an exacerbated NBTI response are obtained, further experiments can be performed to establish the E_{OX}, T, and n dependence on TID and dose-rate effects as demonstrated in the data given in Figure 45.

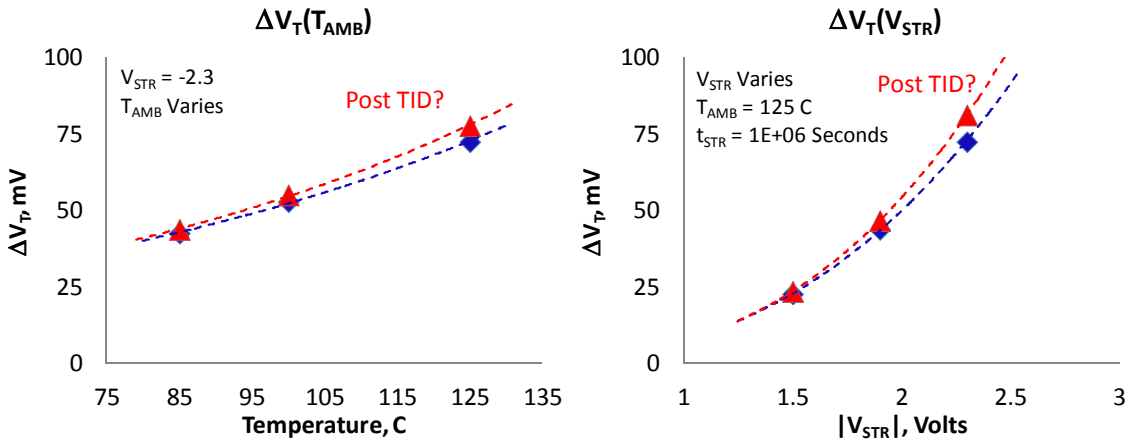

Figure 45. TID effects on NBTI response (notional).

Though others have indicated that BTS instabilities exist as a result of ionizing radiation, none have characterized the extent of the effects within the NBTI framework. The significance of the experiments carried out in this dissertation, is that it sets out to establish to what effect radiation has on the NBTI dependent factors of E_{OX}, T and n.

b. Dose Rate and Total Ionizing Dose Experimental Parameters

Device degradation as a result of exposure to ionizing radiation can potentially be sensitive to the rate the radiation is delivered. In some instances, a particular total dose administered at a dose rate much closer to what the device would see in its operating environment could have a greater effect than if the same total dose were to be administered at a much higher rate.

This phenomenon is known as enhanced low dose rate sensitivity, or ELDRS, and became an issue for bipolar devices [Oldham NSREC 2011 short course] once the semiconductor industry moved from junction to oxide isolation for bipolar devices. Typically, CMOS devices subjected to low dose rate fare as well as the same devices exposed at higher dose rates after being given a proper anneal [38]; however, there may exist a sensitivity to dose rate for NBTI. With a dependence on the outcome of the bias and anneal experiments of the previous section, Table 4 gives the details for the dose-rate sensitivity experiments.

Table 4. Experimental details for dose-rate sensitivity.

Radiation Exper. Cond. & TID Exposure (rad-SiO_2)							Anneal					NBTI Exper. Conditions			
V_{STR} (Volts)	E_{OX} (MV/cm)	T_{amb} (C)	*in situ* Char?	TID (Mrad)	Dur. (Hrs)	Dose Rate (Rad/sec)	V_{STR} (Volts)	E_{OX} (MV/cm)	T_{amb} (C)	*in situ* Char?	Dur. (Hrs)	V_{STR} (Volts)	E_{OX} (MV/cm)	T_{amb} (C)	Dur. (Hrs)
0.0	0.0	25	N	0.7	2	97.2	No Anneal					-2.3	7.2	125	24
0.0	0.0	25	N	0.7	2	97.2	0.0	0.0	25	N	168	-2.3	7.2	125	24
0.0	0.0	25	N	0.7	2	97.2	0.0	0.0	125	N	168	-2.3	7.2	125	24
0.0	0.0	25	N	0.7	24	8.1	No Anneal					-2.3	7.2	125	24
0.0	0.0	25	N	0.7	24	8.1	0.0	0.0	25	N	168	-2.3	7.2	125	24
0.0	0.0	25	N	0.7	24	8.1	0.0	0.0	125	N	168	-2.3	7.2	125	24

From the dose-rate sensitivity experiments, the dependence of ΔV_T and n on post-TID NBTI stresses is evaluated as a function of dose rate for a constant TID. Once dose-rate sensitivity is determined, the experiments can be expanded to investigate the dependence of NBTI degradation as a function of TID given a constant dose rate.

The significance of these experiments is that if it can be shown that NBTI is significantly exacerbated by ionizing radiation via total-dose and dose-rate effects, a mathematical representation can be for the material system under study which describes the relationship between NBTI and ionizing radiation. However, more significantly, the identification of more fundamental processes as work can potentially be made by an evaluation of the data.

c. Synergistic Effects of NBTI and TID

Though the effects of temperature and bias during irradiation and anneal (and to a lesser extent post-anneal BTS effects) on device degradation has been reported in the literature, the combined synergistic effects of NBTI and characterization while being subjected to ionizing radiation has not. With the objective of identifying potential synergistic effects between ionizing radiation and NBTI resulting in accelerated device degradation, Table 5 gives the experimental parameter details for devices subjected to irradiation at different dose rates during a 28-hr NBTI experiment.

Table 5. Experimental conditions of NBTI testing while exposure to irradiation.

Radiation Experimental Conditions for NBTI during TID Exposure						
V_{STR} (Volts)	E_{OX} (MV/cm)	T_{STR} (C)			TID (Mrad) (SiO_2)	
		85	100	125	1.4 (14rad/sec)	2.8 (28rad/sec)
-1.5	4.7			√	√	√
-1.9	5.9			√	√	√
-2.3	7.2	√	√	√	√	√

The focus of this research and reported results pertain to the 14 rad/s regime; while, the 28 rad/s dose rate experiments are the subject on on-going and future work.

C. CONCLUSION

The material system of the p-channel MOSFET has been introduced along with the test methodology and apparatus used to carry out the experiments. Due to a limited knowledge of the material system under study, a number of experiments have been introduced to investigate the p-channel MOSFET NBTI sensitivity to ionizing irradiation under varying conditions with the novel objective of characterizing the device NBTI sensitivity to ionizing radiation. In the chapters that follow the experimental results are presented and discussed.

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IV. NBTI EXPERIMENTAL RESULTS AND ANALYSIS

In this chapter, the process model is first decomposed into the three NBTI dependent parameters of interest: the activation energy E_A; electric-field power-law exponent m; and the stress-time power-law exponent n. The NBTI experimental results are then reported in the context of the process model establishing a baseline of how the devices perform compared to the process model. After which, quantitative analysis is presented assessing the relationship between NBTI resultant changes in device on-current ΔI_{ON} as a function of ΔV_T. The importance of which becomes clear when evaluating the combined ionizing radiation and NBTI effects on the device NBTI performance that is presented and discussed in the subsequent chapters.

A. EVALUATION OF THE PROCESS MODEL

In this section the process model for PMOS NBTI presented in Chapter III is revisited for the purpose of decomposing the model into its three main products for separating the NBTI dependent factors E_A, m, and n. Doing so provides a framework for comparison of the experimentally extracted parametric data to the values of the process model. The process model decomposition is presented first and then followed by the separation of the parameters.

1. Process Model Decomposition

For convenience, the process model introduced in Chapter III is reintroduced here as

$$\Delta V_t = \frac{500 \cdot Z}{500 + Z} = \frac{Z}{1 + \alpha Z} \tag{4.1}$$

where Z is given by

$$Z = A_0 \cdot e^{\frac{-E_A}{k_B T}} \cdot \left(\frac{|V_G|}{T_{OX}} \right)^m \cdot t^n \cdot |V_{T0}|^l \cdot \left[1 + \left(\frac{a_W}{W_D} \right) \right]. \tag{4.2}$$

Because the gate width of the devices under study is sufficiently large, the W_D dependent term approaches unity; and, therefore Equation (4.2) can be written as

$$Z = A_0 \cdot e^{\frac{-E_A}{k_B T}} \cdot \left(E_{OX}\right)^m \cdot \left|V_{T0}\right|^l \cdot t^n. \tag{4.3}$$

Furthermore, Z can be decomposed into

$$Z\left(T, E_{OX}, t, V_{T0}\right) = Z_{E_A}\left(T\right) \cdot Z_m\left(E_{OX}\right) \cdot Z_n\left(t\right) \cdot Z_l\left(V_{T0}\right), \tag{4.4}$$

such that

$$Z_{E_A}\left(T\right) = a_{E_A} \cdot e^{\frac{-E_A}{k_B T}}, \tag{4.5}$$

$$Z_m\left(E_{OX}\right) = a_m \cdot {E_{OX}}^m, \tag{4.6}$$

$$Z_n\left(t\right) = a_n \cdot t^n, \tag{4.7}$$

and

$$Z_l\left(V_{T0}\right) = \left|V_{T0}\right|^l, \tag{4.8}$$

where by A_0 represents the product of the pre-factor terms

$$A_0 = a_{E_A} \cdot a_m \cdot a_n. \tag{4.9}$$

2. Activation Energy

The value of the E_A for NBTI can be experimentally determined by plotting the natural logarithm of the time-to-failure as a function of $1/k_BT$ (Arrhenius plot) for devices stressed at different temperatures to a given failure criteria; where, k_B is Boltzmann's constant in $eV/°K$ and T is the stress temperature in degrees Kelvin. The slope of this line determines the activation energy as shown in Figure 46.

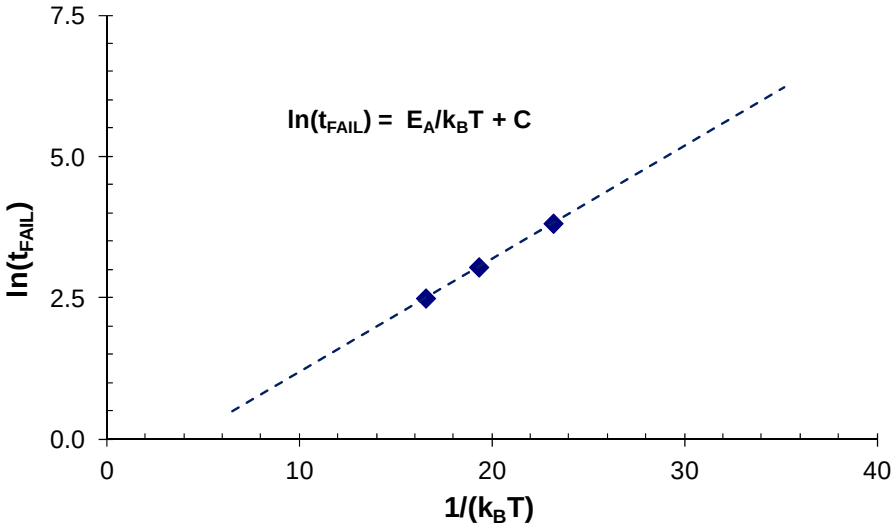

Figure 46. Plot of time-to-failure versus eV^{-1} used to determine the E_A (notional).

In order to determine the E_A using the process model a failure criterion for the ΔV_T is established. To simplify the analysis, the attenuation factor α in Equation (4.1) can be assumed to be very small, such that $1+\alpha Z \approx 1$. Applying the failure criterion and simplification, we can write the process model as

$$\left[\frac{\Delta V_T}{|V_{T0}|}\right]_{CRIT} = \frac{Z_{E_A} \cdot Z_m \cdot Z_n \cdot Z_l}{|V_{T0}|}. \tag{4.10}$$

Since the failure criterion will be met at time t_{CRIT} (or, alternatively, t_{FAIL}) Equation (4.10) can be rewritten, yielding

$$\begin{aligned} Z_n &= |V_{T0}| \cdot \left[\frac{\Delta V_T}{|V_{T0}|}\right]_{CRIT} \cdot \frac{1}{Z_{E_A} \cdot Z_m \cdot Z_l} \\ &= a_n t_{CRIT}^n. \end{aligned} \tag{4.11}$$

Making the proper substitutions for the product terms and solving for t^n, we obtain

$$t_{CRIT}^n = \frac{e^{\frac{E_A}{k_B T}} \cdot E_{OX}{}^{-m} \cdot |V_{T0}|^{-l} \cdot |V_{T0}|}{A_0} \cdot \left[\frac{\Delta V_T}{|V_{T0}|}\right]_{CRIT}. \tag{4.12}$$

Before moving on, it is noted that with this equation along with a prior knowledge of the process model parameters and expected operating stresses (T_{STR} and V_{STR}), a prediction of a given device time-to-failure can be made by taking the n^{th} root of both sides of the equation.

To continue, if it is assumed that the E_{OX} is fixed while T_{STR} is varied, and also assuming for the moment that V_{T0} is temperature invariant, all the terms on the right-hand side of Equation (4.12), with the exception of the temperature-dependent term, can be considered a constant. Therefore, Equation (4.12) can be rewritten as

$$t_{CRIT}^{n} = B_0 \cdot e^{\frac{E_A}{k_B T}} \tag{4.13}$$

in which

$$B_0 = \frac{{E_{OX}}^{-m} \cdot \left|V_{T0}\right|^{1-l}}{A_0} \cdot \left[\frac{\Delta V_T}{\left|V_{T0}\right|}\right]_{CRIT}. \tag{4.14}$$

Taking the natural-logarithm of both sides of Equation (4.13), we get

$$n \cdot \ln\left(t_{CRIT}\right) = \frac{E_A}{k_B T} + \ln\left(B_0\right) \tag{4.15}$$

or, equivalently

$$n \cdot \ln\left(t_{CRIT}\right) = \frac{E_A}{k_B T} + C_0. \tag{4.16}$$

From this equation, and given devices reaching the failure criteria at t_{CRIT} corresponding to a T_{STR}, the activation energy can be empirically determined graphically in a manner similar to Figure 46 or from solving the system of equations:

$$n \cdot \ln\left(t_{CRIT(1)}\right) = \frac{E_A}{k_B T_1} + C_0, \tag{4.17}$$

$$n \cdot \ln\left(t_{CRIT(2)}\right) = \frac{E_A}{k_B T_2} + C_0. \tag{4.18}$$

This yields

$$E_A = n \cdot \ln\left(\frac{t_{CRIT(1)}}{t_{CRIT(2)}}\right) \cdot \left(\frac{T_2 - T_1}{k_B\left(T_2 \cdot T_1\right)}\right). \tag{4.19}$$

The $1/k_BT$ versus $n \cdot \ln(t_{CRIT})$ relationship given various stress temperatures and voltages for a 10% degradation in V_T is illustrated in Figure 47. Recall that n is determined empirically by the slope of the best-fit line by way of the plot of the ΔV_T versus stress-time data plotted on a log-log scale.

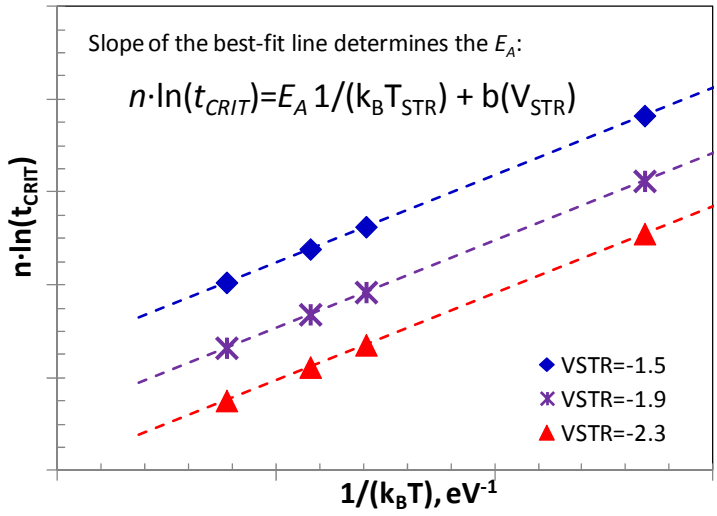

Figure 47. Plot of $n \cdot \ln(t_{CRIT})$ versus eV^{-1} at T_{STR} and V_{STR} to determine E_A.

3. The Electric-Field Power-Law Dependence

Similarly, the electric-field exponent m can be determined given the same failure criteria and resulting time-to-failures. This can be accomplished by holding T_{STR} constant while varying V_{STR}. So doing, assuming all other parameters are E_{OX} invariant, yields

$$t_{CRIT}^{n} = B_0 \cdot E_{OX}^{-m} \tag{4.20}$$

where

$$B_0 = \frac{e^{\frac{E_A}{k_B T}} \cdot |V_{T0}|^{1-l}}{A_0} \cdot \left[\frac{\Delta V_T}{|V_{T0}|} \right]_{CRIT}. \tag{4.21}$$

Therefore, for a given T_{STR} and with knowledge of t_{CRIT} versus V_{STR}, m can be determined experimentally from Equation (4.19) as follows:

$$n \cdot \ln\left(t_{CRIT}\right) = \ln\left(B_0\right) - m \cdot \ln\left(E_{OX}\right)$$
$$= C_0 + m \cdot \ln\left(\frac{1}{E_{OX}}\right). \tag{4.22}$$

As such,

$$n \cdot \ln\left(t_{CRIT(1)}\right) = C_0 + m \cdot \ln\left(\frac{1}{E_{OX1}}\right) \tag{4.23}$$

$$n \cdot \ln\left(t_{CRIT(2)}\right) = C_0 + m \cdot \ln\left(\frac{1}{E_{OX2}}\right) \tag{4.24}$$

which leads to

$$m = n \cdot \ln\left(\frac{t_{CRIT(1)}}{t_{CRIT(2)}}\right) \cdot \ln\left(\frac{E_{OX1}}{E_{OX2}}\right). \tag{4.25}$$

Alternatively, from the plot of $n \cdot \ln(t_{CRIT})$ versus $\ln(1/E_{OX})$, m is given by the slope of the linear fit lines as illustrated in Figure 48, where n is the power law exponent for time.

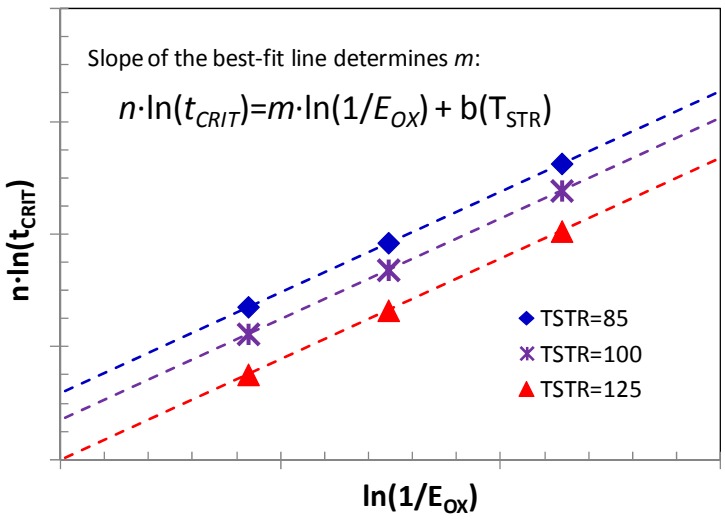

Figure 48. Plot of $n \cdot \ln(t_{CRIT})$ versus $\ln(1/E_{OX})$ to determine m.

4. Stress-Time Power-Law Dependence

Assuming ΔV_T due to NBTI follows a power law, n can be determined by the best fit line of empirical data on a log-log scale, as illustrated in Figure 49.

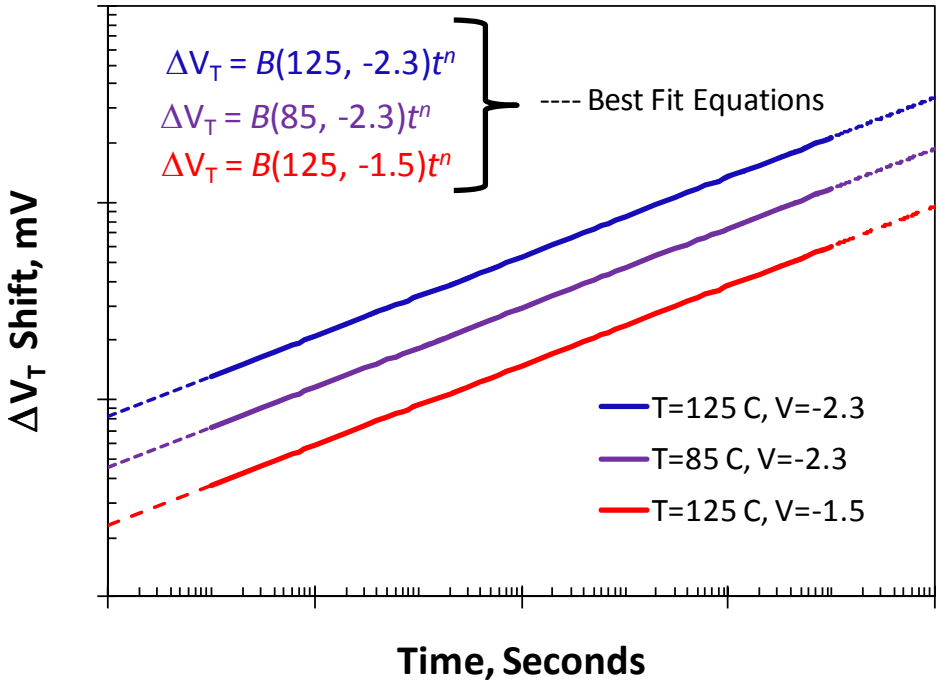

Figure 49. Plot of ΔV_T versus stress time (process model).

As presented previously, and consistent with the plot of Figure 49, the ΔV_T as a function of time takes the form of

$$\Delta V_T = B_0 \cdot t^n, \tag{4.26}$$

in which B_0 is a function of V_{STR} and T_{STR}. For a given V_{STR} and T_{STR} B_0 is a constant. In the case of the process model, assuming again that $\alpha = 0$, ΔV_T is given by

$$\Delta V_T = B_0 \cdot t^n \tag{4.27}$$

in which

$$B_0 = A_0 \cdot e^{\frac{-E_A}{k_B T}} \cdot {E_{OX}}^m \cdot \left|V_{T0}\right|^l. \tag{4.28}$$

Here too, for a given V_{STR} and $T_{STR,}$ B_0 is a constant; as such, n can be written as a function in terms of elapsed stress time and the associated ΔV_T to produce

$$n = \ln\left(\frac{\Delta V_{T1}}{\Delta V_{T2}}\right) \cdot \ln\left(\frac{t_2}{t_1}\right). \tag{4.29}$$

Until this point it has been assumed for simplicity sake that the α term in Equation (4.1) equals zero; however, it is a non-zero, curve-fitting, parameter used to attenuate the growth of the ΔV_T. In the case of this process model, α results in a 2% attenuation per 10 mV of change in threshold voltage. This attenuation also results in a distortion of the time exponent, decreasing the value of n as the stress time progresses. Furthermore, it was assumed that the V_{T0} term is temperature invariant; in actuality it is not and can vary as much as -1 mV/K. The process model does not take this into account. Therefore, future reference to the initial threshold voltage value dependence on ΔV_T will only be reintroduced where warranted by the analysis of experimental data and resulting discussion.

5. Conclusion

In this section, the determination of the E_A, m, and n parameters associated with ΔV_T due to NBTI was presented mathematically and illustrated graphically given the process model. In the section to follow, NBTI experimental data are presented in the context of the process model for the purpose of establishing a valid baseline for the subsequent analysis of the effects of irradiation on the NBTI characteristic parameters of the E_A, m, and n.

B. EXPERIMENTAL PARAMETERS AND CONDITIONS

P-channel MOSFET devices with gate widths of 40 μm and 260 μm and gate length of 0.12 μm underwent NBTI according to the experiment parameters given in Table 6 and the experiment stress and measurement cycles along with bias detail given in Table 7.

Table 6. NBTI experimental parameters applied to PMOS devices under test.

V_{STR} \ T_{STR}	85 C	100 C	125 C
−1.5 V			√
−1.9 V			√
−2.3 V	√	√	√

Table 7. Experiment stress and measurement cycles with device bias detail.

Parameter	Description	Value	Units
t_{DUR}	Experiment Duration	~25	hrs
		~86,400	s
τ_{STR-i}	Initial Stress Interval	600	s
τ_{STR-2}	Second Stress Interval	3000	s
τ_{STR}	Subsequent Stress Intervals	3600	s
τ_{MEA}	Measure Interval	150	s
V_G	Gate Bias	V_{STR}	V
V_S	Source Bias	0	V
V_D	Drain Bias	0	V
V_B	Bulk/n-Well Bias	0	V
V_{SUB}	Substrate Bias	0	V

The stress-measure-stress cycle management, control of the stress and measure bias, *I-V* sweeps, and raw data collection was performed by an automated test program on the Keithley 4200-SCS platform. The test program flow is presented in Figure 50.

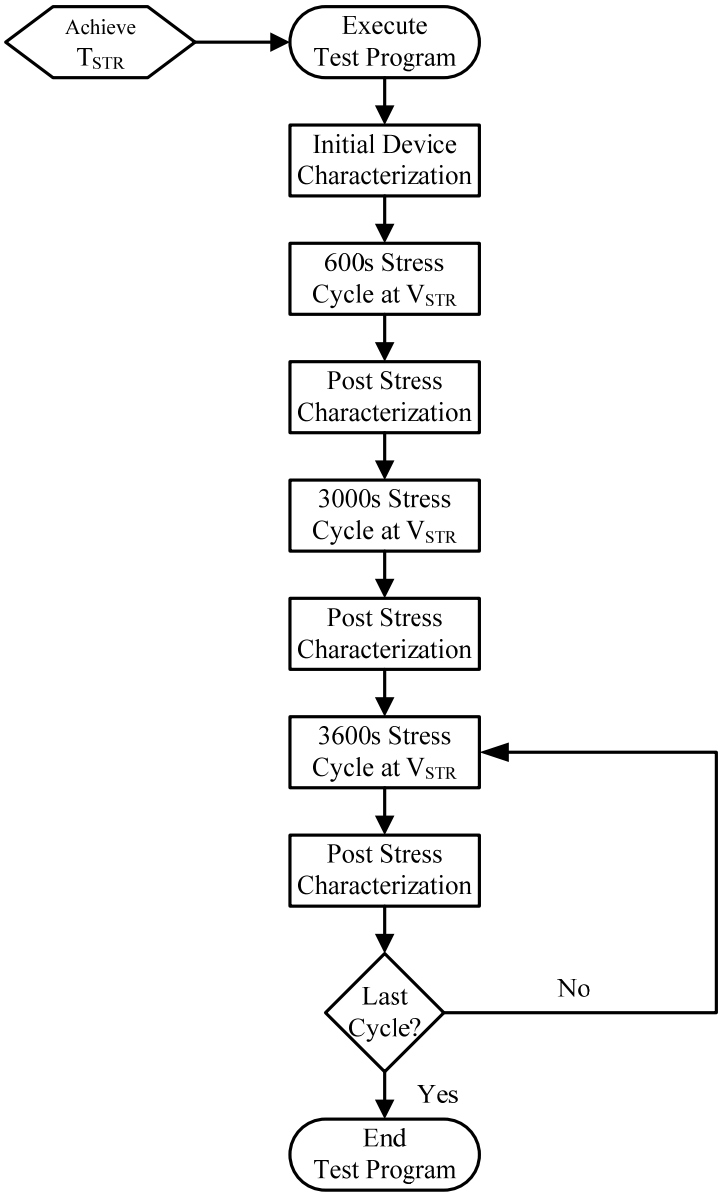

Figure 50. Keithley test program flow for NBTI characterization.

In general, experiments began with an initial device characterization at the specified stress temperature, and then proceeded with a series of stress-measure-stress cycles for the duration of the experiment. During each measurement cycle, the gate stress was removed and the test program executed I_D-V_D, and I_D-V_G sweeps in the linear and saturation regions of operation collecting data for evaluation of, and changes in, the V_T, I_{ON}, g_m, and μ_{eff} (or, μ_p in the case of the PMOS transistor) parameters. The bulk of the data post-processing was performed in MATLAB. Figure 51 illustrates the applied

voltage sequence to the gate during the measurement cycles; the importance of which, in the context of the NBTI recoverable component, will be shown later during the discussion of the NBTI results and analysis.

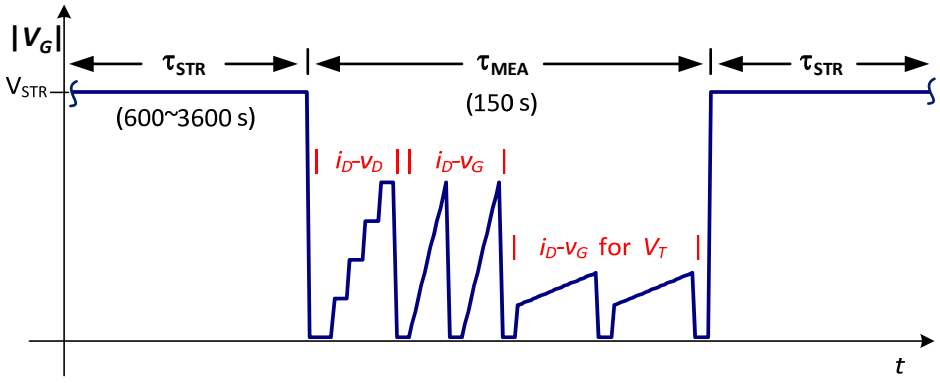

Figure 51. Applied gate voltage during measurement sequence.

With four devices per packaged part being experimented on simultaneously, each device in turn was sequentially removed from stress periodically for characterization while leaving the other devices in stress mode as graphically illustrated in Figure 52. This was carried out by the Keithley's four available source measurement units (SMUs) and integrated Keithley 707A switch matrix.

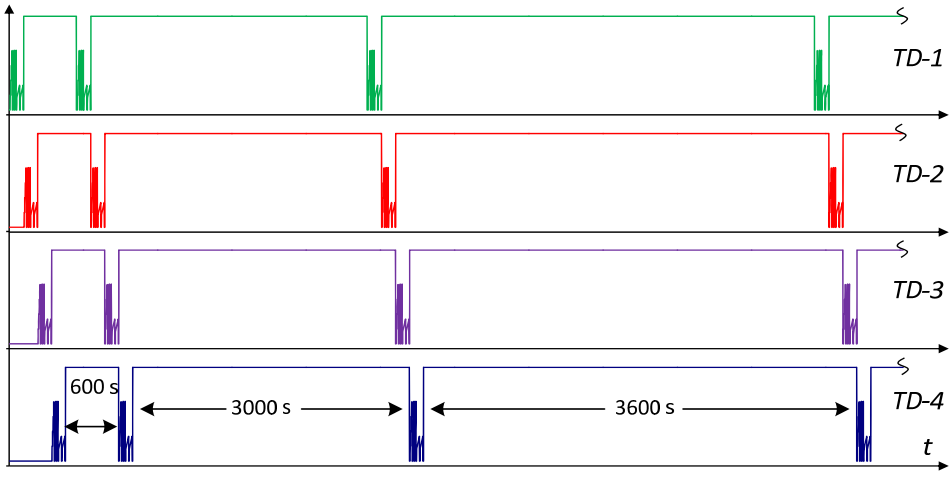

Figure 52. Graphical illustration of sequential stress-measure-stress cycles.

C. NBTI EXPERIMENTAL RESULTS AND ANALYSIS

Experimental data was collected over the various stress conditions and changes in V_T as a function of stress time was captured for characterizing the n, E_A, and m parameters using regression analysis. The results of which, beginning with the power-law exponent for time, followed by the activation energy, and concluding with the power-law exponent for the electric field are presented. After which, for comparative purposes, the experimental results for the I_{ON} are presented.

1. Experimental Results for ΔV_T

In the section to follow, the experimental results obtained from ΔV_T as a function of T_{STR} and V_{STR} are presented in terms of n, E_A and m.

a. Time-Dependent Power-Law Exponent, n

The plots of Figure 53 and Figure 54 present n as a function of V_{STR} (E_{OX}) and T_{STR}, respectively. Both plots give n as approximately 0.255 for the experimental data, which was consistent with the process model. The difference between the experimental data versus the process model can be attributed to likely differences in the measurement techniques used in characterizing the devices, test article preparation, and the test equipment used. As was expected, n was shown to be a relatively constant value demonstrating it is independent of both stress temperature and voltage. For the data in Figure 53, dispersion was noted at the low V_{STR} point and is attributed to a relatively small ΔV_T compared to experiments conducted at higher stresses. Furthermore, the value of n obtained experimentally is consistent with that which has been reported in the literature. More importantly, the objective of establishing a baseline from which *in situ* irradiation and post-TID NBTI results can be compared was achieved.

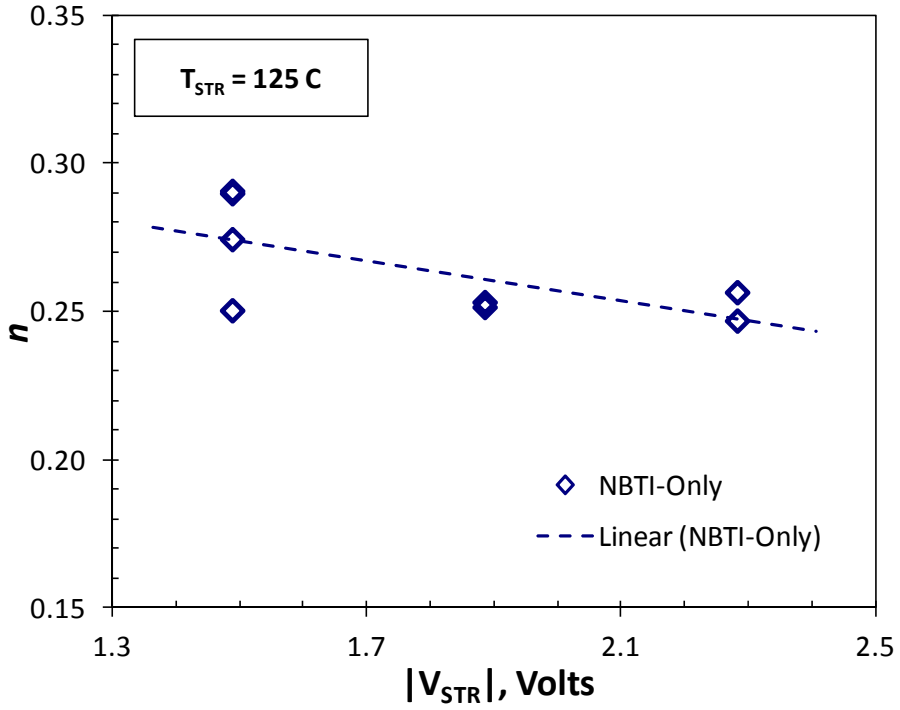

Figure 53. Power-law exponent for time n versus V_{STR}.

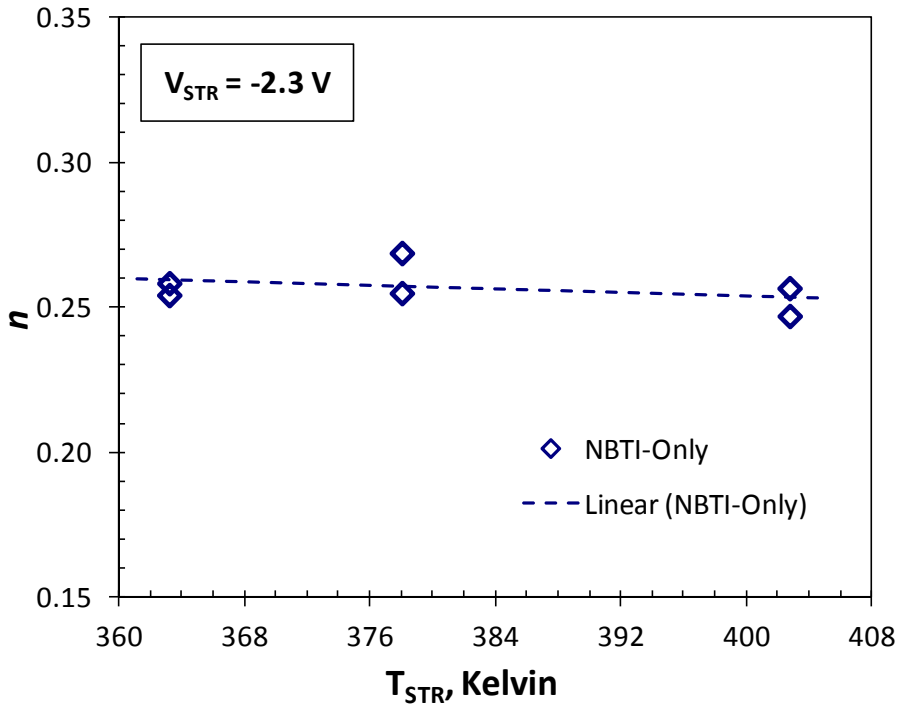

Figure 54. Power-law exponent for time n versus T_{STR}.

b. Temperature-Dependent Activation Energy E_A

The temperature-dependent activation energy is given by the slope of the linear regression line presented in Figure 55 where *n* is the exponent for time. From the experimental data E_A = 0.35. Again, differences between the experimental data and the process model can be attributed to differences in the measurement techniques used in characterizing the devices, test article preparation, and the test equipment used.

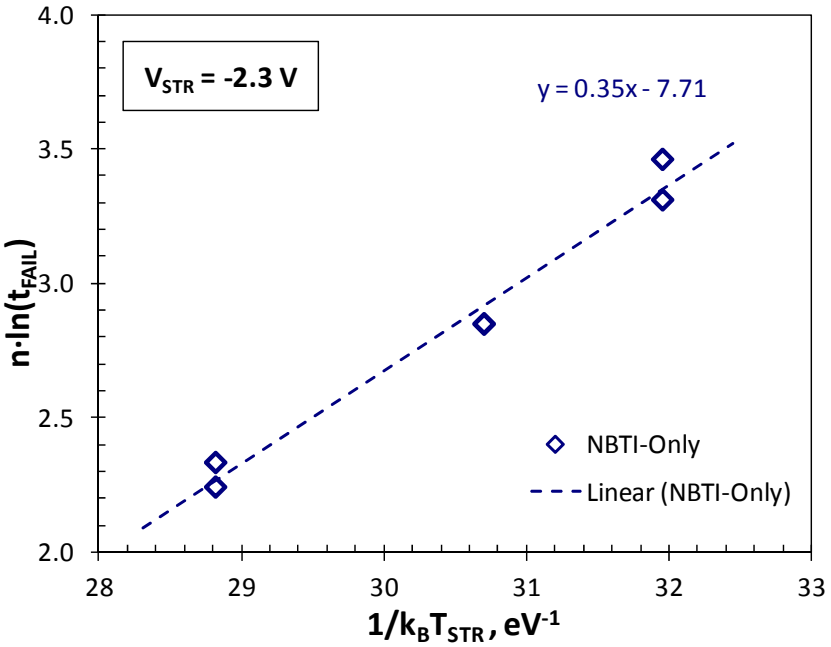

Figure 55. Extraction of the thermal activation energy E_A.

c. Electric Field-Dependent Power-Law Exponent, m

The power-law exponent *m* is given by the slope of the best-fit line in the plot of Figure 56. For the experimental data, *m* = 5.0 and was consistent with the process model considering the potential differences measurement technique and other factors as described previously.

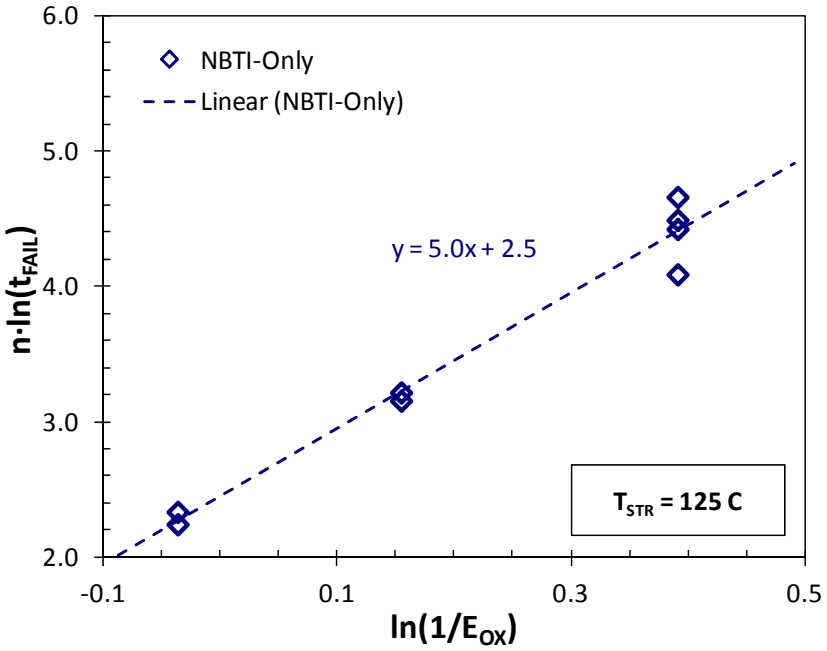

Figure 56. Extraction of the power-law exponent m for E_{OX}.

d. Summary

From the regression analysis of the experimental data collected on the ΔV_T, the n, E_A, and m parameters were extracted establishing a baseline from which a comparative analysis can be performed on irradiated devices undergoing the same NBTI experiments.

2. Experimental Results for ΔI_{ON}

The transistor drive-current I_{ON} defined as the I_{DS} measured under the condition for which $V_{GS} = V_{DS} = V_{DD}$ while $V_B = V_S = 0$ V, was characterized in a similar manner to ΔV_T for assessing the NBTI related degradation of I_{ON}, ΔI_{ON}. Again, the temperature, field, and power-law dependent parameters n, E_A and m, respectively were extracted from the raw experimental data via MATLAB.

a. Power-Law Exponent n for Time-Dependent Degradation

The plots of Figure 57 and Figure 58 give the power-law exponent for the time-dependent degradation of I_{ON} as related to V_{STR} and T_{STR}, respectively. Here too, n appears to be independent of V_{STR} and T_{STR} given the relatively flat (zero slope) response.

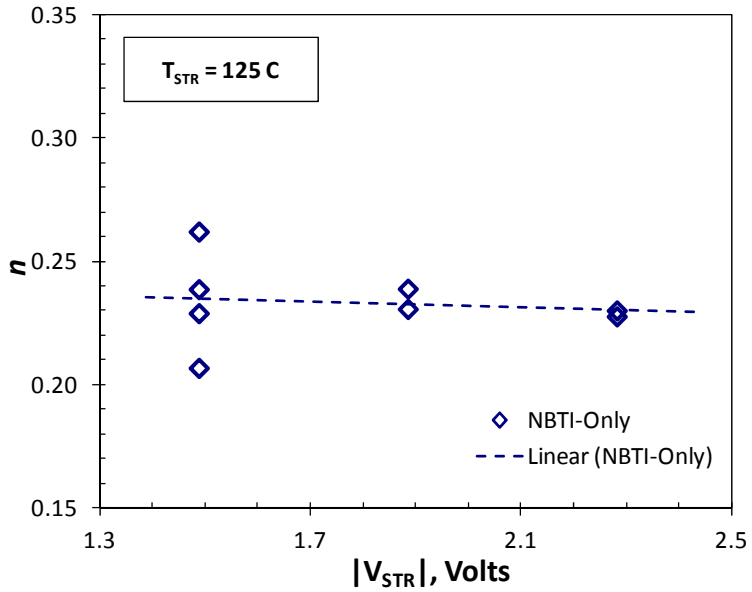

Figure 57. Power-law exponent n vs. V_{STR} for ΔI_{ON}.

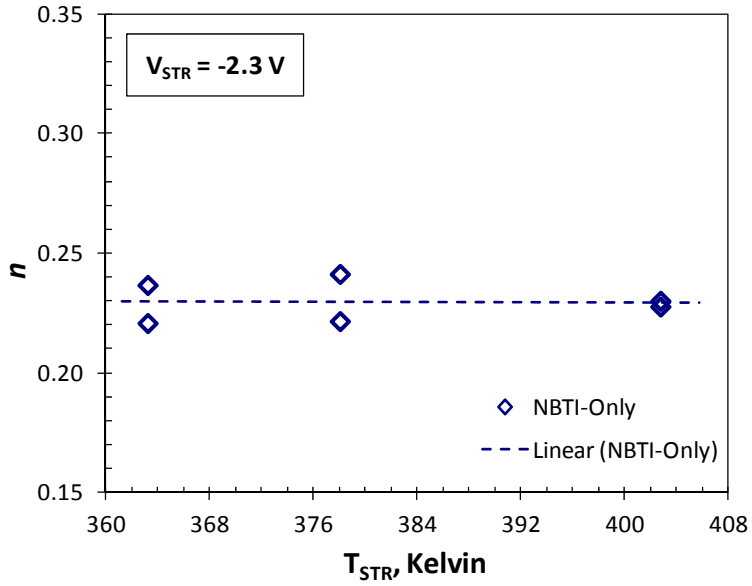

Figure 58. Power-law exponent n vs. T_{STR} for ΔI_{ON}.

b. Temperature-Dependent Activation Energy, E_A

As was the case for the activation energy associated with ΔV_T as a function of T_{STR}, the activation energy associated with ΔI_{ON} as a function of T_{STR} is illustrated by the slope of the line given in the plot of Figure 59.

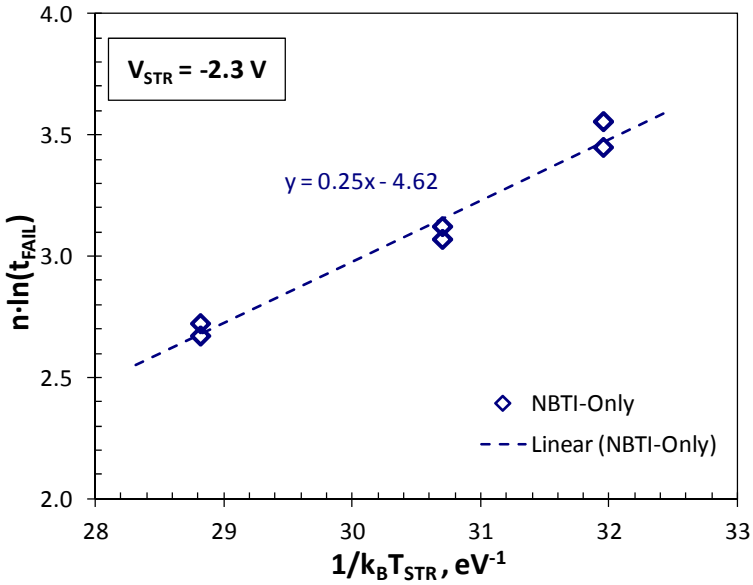

Figure 59. Thermal activation energy E_A via the slope of $n \cdot ln(t_{FAIL})$ vs. $1/k_BT$ for ΔI_{ON}.

c. Electric-Field Dependent Power-Law Exponent, m

The power-law exponent for ΔI_{ON} is given by the slope of the best-fit line of Figure 60.

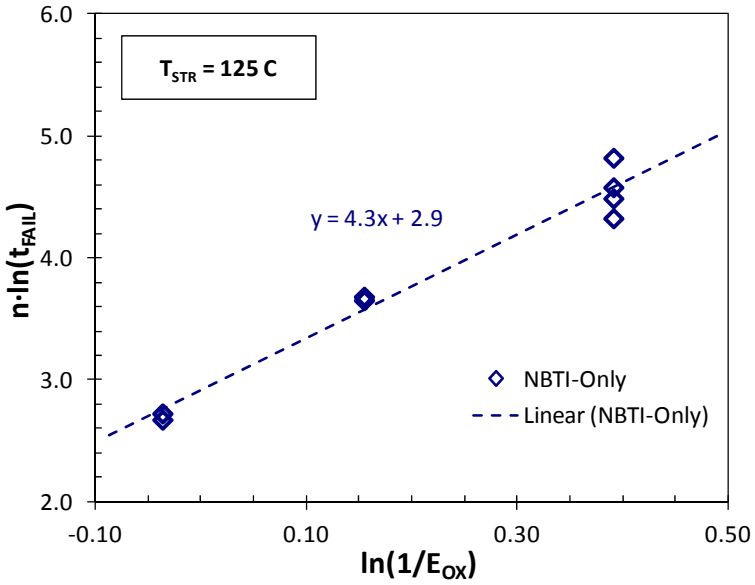

Figure 60. Electric-field E_{OX} dependence of ΔI_{ON} to NBTI.

3. Summary of Results

The n, E_A and m parameters extracted from the experimental data for ΔV_T and ΔI_{ON} due to NBTI are summarized in Table 8.

Table 8. Summary of NBTI degradation parameters for ΔV_T and ΔI_{ON}.

Parameter	n	E_A	m
ΔV_T	0.26	0.35	5.0
ΔI_{ON}	0.23	0.25	4.3

There is relatively close agreement between the parameters for ΔV_T and ΔI_{ON} which is to be expected due to the relationship between I_{DS} and V_T given by

$$I_{DS} = \frac{1}{2}\mu_p C_{OX}\frac{W}{L}\left(V_{GS} - V_T\right)^2. \tag{4.30}$$

In the section to follow, the interdependence between ΔV_T and ΔI_{ON} is discussed.

D. QUANTITATIVE ANALYSIS OF ΔV_T AND ΔI_{ON}

This section deals with the relationship between the stress-induced changes to V_T and I_{ON} as a function of stress time. The discussion begins with the measurement methods used and their validity in obtaining I_{ON} and V_T. This is then followed by a presentation of the experimental data that demonstrates the dependency of ΔI_{ON} on ΔV_T. This section, with the use of the ideal MOSFET equation for I_{DS} in the saturation region of operation, then concludes with a mathematical representation of the ΔI_{ON}-ΔV_T relationship; the result of which supports the experimental findings presented.

1. Measurement Methods of Obtaining V_T and I_{ON}

As presented in the previous section, stress-induced changes in V_T and I_{ON} were captured as a function of stress time. From these data, the time-, electric field-, and temperature-dependent parameters were extracted and summarized. To recall, I_{ON} was defined as the drain current measured given the condition $V_{GS} = V_{DS} = V_{DD}$ while $V_B = V_S = 0$ V. Under these conditions, the I_{ON} data were extracted from the I_{DS}-V_{DS} sweeps

recorded during the measurement periods of the stress-measure-stress cycles of the NBTI experiments carried out under the various temperature and stress voltage conditions.

In extracting V_T, a constant drain current method (or simply, constant-current method) was employed in which, with the transistor biased in the forward-active region ($V_{DS} >> V_{GS} - V_T$), a voltage was applied to the gate terminal and incremented until a desired drain current $I_{D\text{-}CC}$ was achieved. Under this method, the threshold voltage is then defined as the applied gate voltage needed to achieve $I_{D\text{-}CC}$. The constant-current method is a valid approach for extracting V_T provided that the stress-induced changes in V_T which necessitate a change in V_G to maintain $I_{D\text{-}CC}$ are only a result of changes to the V_T and not as a result of changes in the channel mobility parameter, μ_p. The tell-tale signature of whether a change in I_{DS} is a function of ΔV_T or $\Delta\mu_p$ is demonstrated graphically in the I_{DS}-V_G plots of Figure 61.

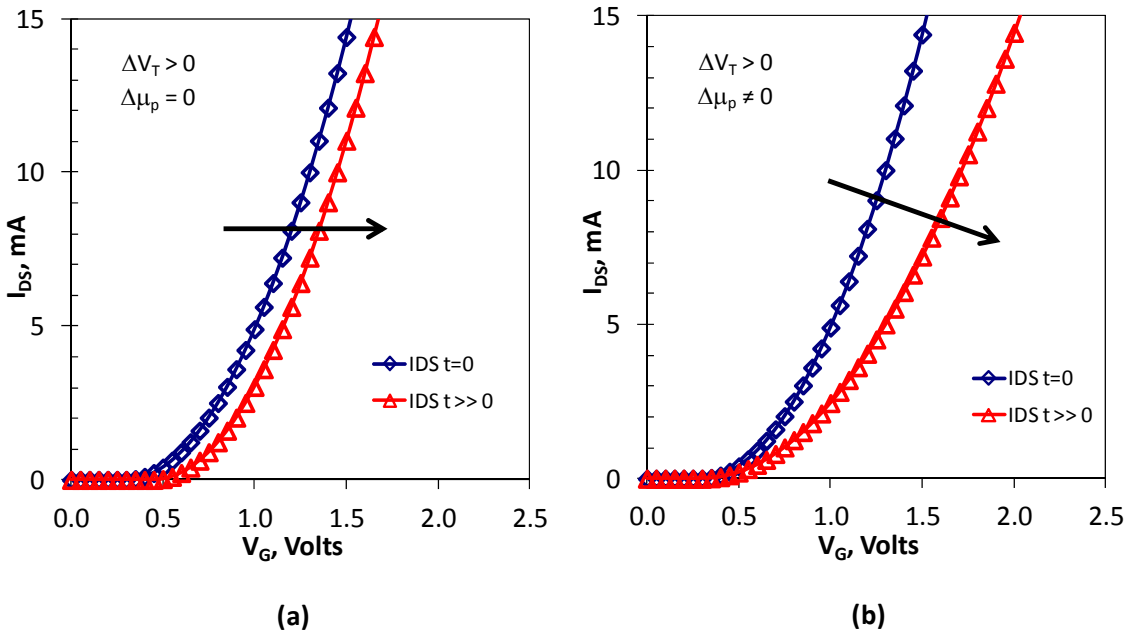

Figure 61. I_{DS}-V_G plot demonstrating the effects of (a) ΔV_T and (b) $\Delta\mu_p$ on I_{DS}.

A pure horizontal translation in I_{DS} vs. V_G is indicative of a change in I_{DS} due to ΔV_T as shown in Figure 61(a); whereas, (b) demonstrates, in addition to a possible horizontal translation, a change in the slope of the I_{DS}-V_G curve indicating a change in the

μ_p. This graphical representation of horizontal translation and change of slope is also evident in the ideal equation for I_{DS} given by

$$I_{DS} = \frac{1}{2}\mu_p C_{OX}\frac{W}{L}\left(V_{GS} - V_T\right)^2, \tag{4.31}$$

in which the μ_p affects the steepness of the curve in the region where $V_{GS} > V_T$ and the V_T affects the horizontal position. The analysis of the I_{DS}-V_G data for devices subjected to NBTI was characteristic of Figure 61(a); therefore, it was assumed that $\Delta\mu_p$ effects were minimal compared to the effect of ΔV_T on I_{DS} and thereby demonstrating the constant-current method valid for determining stress-induced ΔV_T.

2. Comparison of ΔI_{ON} vs. ΔV_T

Devices were subjected to the NBTI stress-measure-stress routine with the voltage-temperature combinations given in Table 9. The V_T and I_{ON} were logged versus stress time.

Table 9. Experimental stress combinations for NBTI characterization.

T_{STR} / V_{STR}	85 C	100 C	125 C
−1.5 V			√
−1.9 V			√
−2.3 V	√	√	√

For each stress condition a separate characteristic equation was derived from the experimental data. After which, the per cent degradation of V_T and I_{ON} could be expressed as a function of stress time. For the experiments performed, the per cent degradation of V_T and I_{ON} was established at a stress time of 80×10^3 seconds. The results of which are given in Figure 62.

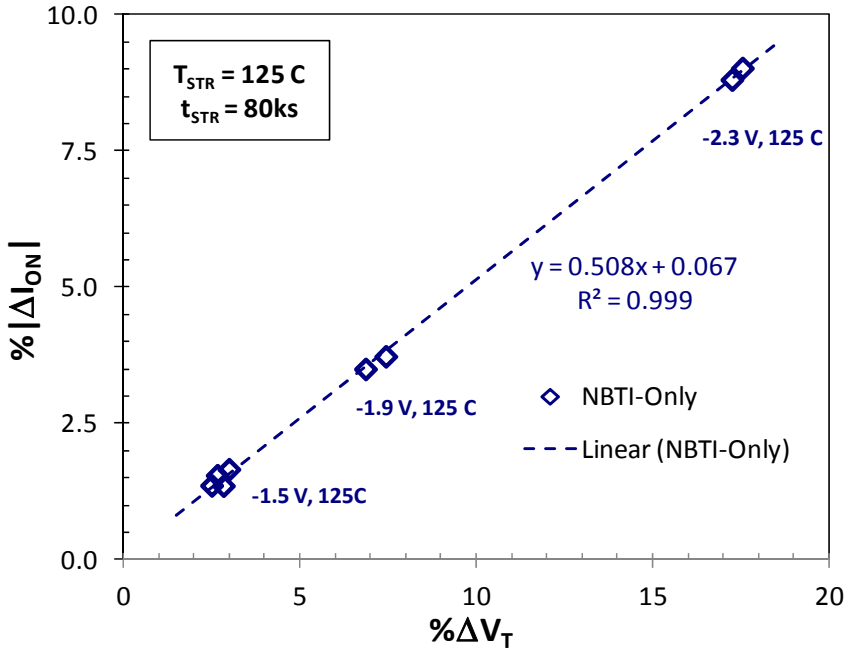

Figure 62. Plot of $\%|\Delta I_{ON}|$ vs. $\%\Delta V_T$.

The dependence of ΔI_{ON} on ΔV_T was established through regression analysis of the data which exhibits a linear relationship. As a result, the ideal form of the I_{DS} equation in the saturation region of operation can be shown to a first-order approximation to express the relationship between changes in I_{ON} and V_T mathematically. The derivation of this relationship follows.

Starting with Equation (4.31) evaluated at $V_{GS} = V_{DS} = V_{DD}$, we obtained

$$I_{ON} = K_P \left(V_{DD} - V_T \right)^{\beta} \tag{4.32}$$

where

$$K_P = \frac{1}{2} \mu_P C_{OX} \frac{W}{L}, \text{ and } 1 \le \beta \le 2. \tag{4.33}$$

In the long-channel form of Equation (4.32), β approaches two. As short channel effects typical of deep submicron devices begin to manifest, β tends toward unity. Continuing on, it is desired to evaluate the change in I_{ON} with respect to change in the V_T and express ΔI_{ON} in terms of ΔV_T; therefore the fractional change in ΔI_{ON} can be expressed as

$$\frac{\Delta I_{ON}}{I_{ON-0}} = \frac{K_P\left[\left(V_{DD}-V_{T0}\right)^{\beta} - \left(V_{DD}-\left(V_{T0}+\Delta V_T\right)\right)^{\beta}\right]}{K_P\left(V_{DD}-V_{T0}\right)^{\beta}}. \tag{4.34}$$

Again, assuming that the primary contribution to ΔI_{ON} is ΔV_T with $\Delta\mu_p$ being negligible, we can rewrite Equation (4.34) as

$$\frac{\Delta I_{ON}}{I_{ON-0}} = \frac{\left(V_{DD}-V_{T0}\right)^{\beta} - \left(V_{DD}-\left(V_{T0}+\Delta V_T\right)\right)^{\beta}}{\left(V_{DD}-V_{T0}\right)^{\beta}},$$

$$= 1 - \frac{\left(V_{DD}-\left(V_{T0}+\Delta V_T\right)\right)^{\beta}}{\left(V_{DD}-V_{T0}\right)^{\beta}},$$

$$= 1 - \left[\frac{V_{DD}-V_{T0}-\Delta V_T}{V_{DD}-V_{T0}}\right]^{\beta}, \tag{4.35}$$

$$= 1 - \left[1 - \frac{\Delta V_T}{V_{DD}-V_{T0}}\right]^{\beta}.$$

Since the ΔV_T term is small compared to the $V_{DD} - V_{T0}$ term, the ratio of the two terms is small; therefore, using the binomial expansion

$$\left(1 \pm \alpha\right)^{\beta} \simeq 1 \pm \beta\alpha, \text{ for } \alpha \ll 1, \tag{4.36}$$

we can rewrite Equation (4.35) as,

$$\frac{\Delta I_{ON}}{I_{ON-0}} = 1 - \left(1 - \beta\frac{\Delta V_T}{V_{DD}-V_{T0}}\right),$$

$$= \frac{\beta}{\left(\frac{V_{DD}}{V_{T0}}-1\right)}\frac{\Delta V_{T0}}{V_{T0}}. \tag{4.37}$$

Substituting reasonable values for V_{T0}, β, and V_{DD} of 0.3 V, 1.6, and 1.2 V, respectively, we get

$$\frac{\Delta I_{ON}}{I_{ON-0}} = 0.533 \frac{\Delta V_T}{V_{T0}}. \tag{4.38}$$

This result is in relatively close agreement to the plot of the best fit line of the experimental data presented in Figure 62. Having established the fractional change in I_{ON} was linearly proportional to the fractional change in V_T leads to the expression

$$\frac{\Delta I_{ON}}{I_{ON-0}} = \frac{\beta}{\left(\frac{V_{DD}}{V_{T0}} - 1\right)} \cdot A_{V_T}\left(V_{STR}, T_{STR}\right) t^{n_{V_T}}. \tag{4.39}$$

This result suggests that changes in I_{ON}, at least for the technology under evaluation, should follow the same power law and stress dependencies as V_T. As previously revealed there was a small difference in the experimental means for n_{VT} and n_{ION}. In exponential terms the difference is small yet quantifiable. One possible explanation for the difference could involve the fact there was a significant time lag (~60 seconds) between the measurements of I_{ON} and V_T. This would allow more recovery to take place resulting in a skewing of ΔV_T, the result being a slightly higher value for n.

3. Summary

Examination of the experimental data established the dependence of ΔI_{ON} on ΔV_T. This dependence was substantiated in mathematical terms using the ideal MOSFET equation for I_{DS} yielding the relationship

$$\frac{\Delta I_{ON}}{I_{ON-0}} = \frac{\beta}{\left(\frac{V_{DD}}{V_{T0}} - 1\right)} \cdot \frac{\Delta V_T}{V_{T0}}. \tag{4.40}$$

This result demonstrated that the observed changes in I_{ON} were due primarily to changes in V_T and served to substantiate the constant-current method for extracting V_T.

E. CONCLUSION

In this chapter on the NBTI experimental results and analysis, the process model for NBTI was re-introduced, decomposed, and separated out into the NBTI parameters of interest (n, E_A and m) both graphically and analytically. This progression established a framework from which to process and compare the experimental results. After an introduction to the NBTI experimental parameters and conditions, including the timing sequence of the measurement cycles, the discussion moved to the experimental results.

Though the NBTI parameters extracted from the experimental data differed somewhat from those of the process model, they were none-the-less deterministic and quantifiable. More importantly, the experimental results established a baseline whereby a comparative analysis could be performed between ΔI_{ON} and ΔV_T. That analysis demonstrated, both graphically and quantitatively, the relationship between ΔI_{ON} and ΔV_T (or, more specifically, the dependence of ΔI_{ON} on ΔV_T). The resulting framework and experimental baseline established in this chapter to analyze NBTI in PMOS devices can now be extended to evaluate the effects of ionizing radiation on the NBTI characteristics in these devices—the subject of the following chapter.

V. COMBINED EFFECTS RESULTS AND ANALYSIS

In this chapter, the results from the combined effects experiments are presented and compared to the results of the NBTI characterization presented in the previous chapter. The results for devices subjected to irradiation prior to NBTI will be presented first, followed by the results for devices subjected to irradiation while undergoing NBTI. It will be demonstrated that ionizing radiation alters the PMOS device response to NBTI thus altering the NBTI characteristics. These manifested most notably as the fractional change in the ΔI_{ON} versus ΔV_T relationship suggesting an increased involvement of interface states as a result of the irradiation. Furthermore, at operationally relevant NBTI stress conditions, NBTI was enhanced; whereas, under the highest-stress conditions a decrease in NBTI was observed. The chapter concludes with an empirical model accounting for the irradiation induced changes.

A. RADIATION FOLLOWED BY NBTI

In this section on post-TID NBTI characterization, the experiment and experimental results of devices subjected to 0.7 Mrad(SiO_2) ionizing radiation, anneal, and NBTI stresses, are discussed. Though the experiments were designed to establish device NBTI sensitivities to dose-rate and anneal conditions, no such sensitivity was apparent. Post-irradiation NBTI characterization and analysis revealed that the overall NBTI response was attenuated at the highest stress condition for V_{STR} and T_{STR} compared to their NBTI-only counterparts. The significance of that result is that it was repeated in the devices subjected to irradiation during NBTI. The fact that similar outcomes were achieved at the high-stress condition suggests that the NBTI attenuation was not dependent on whether or not the devices were subjected to NBTI and irradiation concurrently.

1. Experimental Setup

PMOS devices were selected from the same wafer as the devices selected for the NBTI-only experiments and were packaged in a similar manner. In order to investigate the NBTI sensitivity to irradiation and anneal, the devices were subjected to zero-bias,

room-temperature, irradiation to 0.7 Mrad(SiO_2) at either 8.1 or 97.2 rad/s followed by either direct NBTI or a 168-hr anneal at 25 or 125 C prior to NBTI as outlined in the flow diagram of Figure 63.

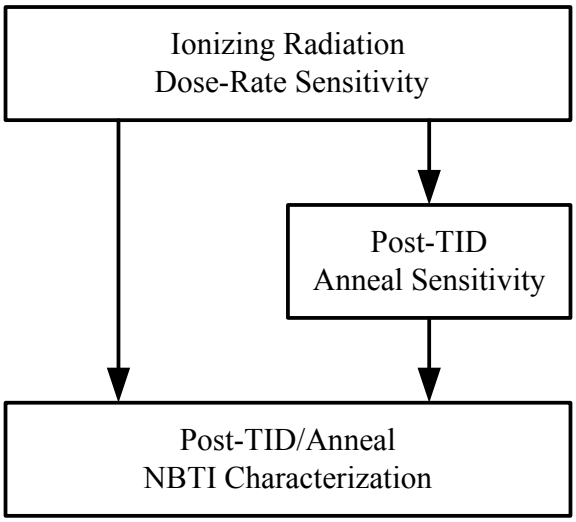

Figure 63. Post-TID NBTI characterization flow.

For the purpose of tracking irradiation and anneal dependent changes in the device characteristics, the devices were characterized before and after irradiation and post-anneal prior to the NBTI for NBTI characterization.

2. Experimental Results and Analysis

Since these devices were limited to a single NBTI stress point (-2.3 V, 125 C) a complete characterization to establish the temperature and electric field dependent parameters was not performed nor was a complete comparison made to the NBTI-only experiments. However, a comparison to devices receiving similar stresses was made. As mentioned previously, irradiated devices subjected to the high-stress condition (-2.3 V, 125 C) consistently demonstrated an attenuated NBTI response to NBTI stress. Also observed was an increase in the ratio of fractional ΔI_{ON} to ΔV_T suggesting an increase in interface trap density. Furthermore, it was observed that though there was increased variability, or dispersion, in the n_{ION} and n_{VT} time exponents, the average values of n_{ION} and n_{VT} remained unchanged compared to the NBTI-only devices suggesting ionizing

radiation prior to NBTI does not have an effect on the time dependent processes responsible for the NBTI. There was no correlation observed between the ΔV_T and the method of anneal or dose rate. Bias sensitivities were not investigated. A detailed comparative analysis of devices irradiated prior to NBTI is included in the following section on concurrent radiation and NBTI.

B. CONCURRENT RADIATION AND NBTI

To date, the combined effects of ionizing radiation and NBTI on PMOS devices have not been reported in the literature. In this section, the results of the combined effects experiments are presented demonstrating ionizing radiation do have an effect on PMOS NBTI. It is shown, through the results and analysis of the fractional change of ΔI_{ON} versus ΔV_T data, that for operationally relevant conditions for T_{STR} and V_{STR}, NBTI was enhanced in the presence of ionizing radiation; whereas, under high V_{STR} NBTI was attenuated. In the discussion that follows, the experimental results and analysis are presented.

1. Experimental Setup

P-MOSFET devices packaged identically to those of the NBTI-only experiments were subjected to 14 rad/s ionizing radiation. Data was collected using the same Keithley 4200-SCS test and data acquisition program utilized in the NBTI-only experiments and the data analysis was performed in the same manner for a direct comparison of the results.

2. Experimental Results for ΔV_T

The results of the combined effects experiments, as compared to the NBTI-only results, are presented. Values for n, E_A and m were extracted. Potential changes in these NBTI parameters were observed. The differences between the NBTI-only versus the NBTI in the presence of gamma-ray irradiation NBTI+γ were not significant enough to make conclusive judgments about changes to n, E_A and m. The experimental results follow.

a. Time-Dependent Power-Law Exponent, n

The time exponent n for the results of the NBTI and NBTI+γ experiments is given in Figure 64. The left side plot of the Figure 64 gives n as a function of T_{STR} whereas the plot on the right represents n as a function of V_{STR}.

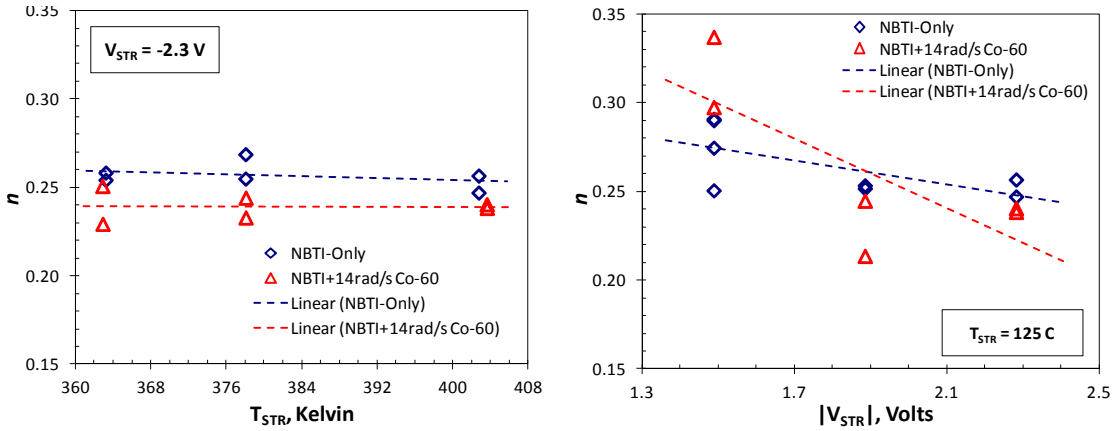

Figure 64. Plot of n versus T_{STR} (left) and V_{STR} (right) for ΔV_T.

For NBTI in general, it has been well established that n is independent of T_{STR} or V_{STR}. This independence was reflected in the process model and, with minor deviation, the actual NBTI-only results as well. The value of n = 0.255 for ΔV_T is consistent with what has been reported in the literature for the SMS method of NBTI characterization where the delay between the removal of the stress and measurement allows for the recovery of the recoverable component of NBTI.

For NBTI characterization methods where the stress-to-measure delay is minimized to minimize the recoverable component of NBTI, such as the OTF or an ultra-fast OTF method, the value of n approaches 1/6. With the introduction of ionizing irradiation to the NBTI stress it was also observed that for ΔV_T versus T_{STR} n was slightly reduced compared to the NBTI-only results.

According to the R-D theory presented in Chapter II, n is related to the rate hydrogen dissociates from and diffuses away from the Si-SiO_2 interface into the gate oxide. For the switched-trap model, also presented in Chapter II, n is the rate hydrogen

dissociates from the Si-SiO_2 interface as result of a channel hole tunneling into the oxide and becoming trapped at an oxygen vacancy or E′-center. This hole-trapping event results in the structural relaxation of the weak Si-Si bond leaving an unpaired electron on one of the Si atoms. This in turn leads to a thermodynamic unstable condition whereby the hydrogen used to passivate the Si dangling bonds at the Si-SiO_2 interface can dissociate from the interface in favor of bonding with the nearby unpaired electron of the E′-center thereby creating an interface state at the interface from which the hydrogen originated.

During irradiation, electron-hole pairs are created. In the presence of an electric field these charges are separated where holes drift toward the gate-terminal and electrons drift toward the channel where they can recombine with channel holes. The switch-trap models given by Grasser and Lelis allow for a process in which the positive E′-center trap can undergo hole-emission (electron capture) creating a charge neutral defect referred to as a neutral electron trap, or NET. This would have the effect of reducing the ratio of hole traps in the oxide to interface traps at the interface, thereby altering the processes responsible for NBTI.

b. Temperature-Dependent Activation Energy, E_A

The experimental results of the NBTI related activation energy is presented in Figure 65. The data points represent the projected TTFs as a function of $1/T_{STR}$ for a constant V_{STR}, and therefore, the slopes of the linear-fit lines represent the E_A.

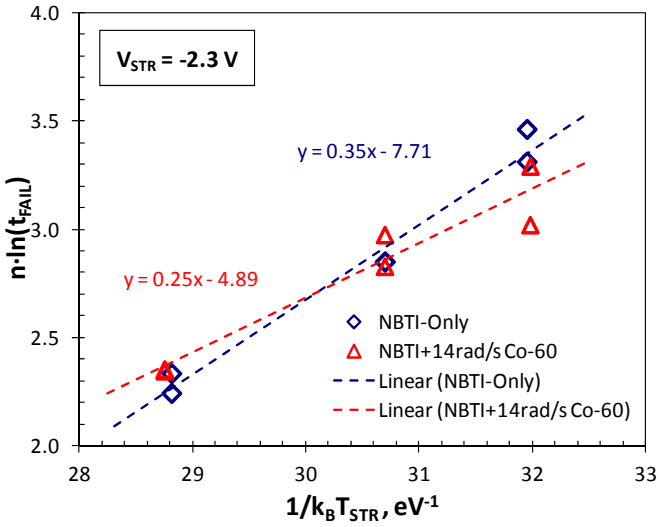

Figure 65. Determining the thermal activation energy E_A for ΔV_T.

Due to sensitivity inherent in the calculation of the TTF projections and the dependence of the extracted value on n

$$E_A = n \cdot \ln\left(\frac{t_{CRIT(1)}}{t_{CRIT(2)}}\right) \cdot \left(\frac{T_2 - T_1}{k_B\left(T_2 \cdot T_1\right)}\right), \tag{5.1}$$

the experimental data suggests that ionizing radiation did not have an influence on the E_A. Therefore, the experimentally determined value for E_A can be considered comparable to the process model; however, the TTFs for the NBTI-only and NBTI+γ were demonstrably better than the process model (not shown) revealing the statistical worse-case nature of the process model with regard device lifetimes.

The addition of ionizing radiation to the NBTI does not appear to have a significant effect on E_A indicating no additional sensitivity of ΔV_T to T_{STR} as a result of ionizing radiation. This finding was consistent with that of the time exponent for constant V_{STR}.

c. Electric Field-Dependent Power-Law Exponent, m

The slopes of the best-fit lines given in the plots of Figure 66 represent the power-law exponent m for field dependence. For ΔV_T, no significant change in the electric field-dependence was observed between the NBTI-only and NBTI+γ results.

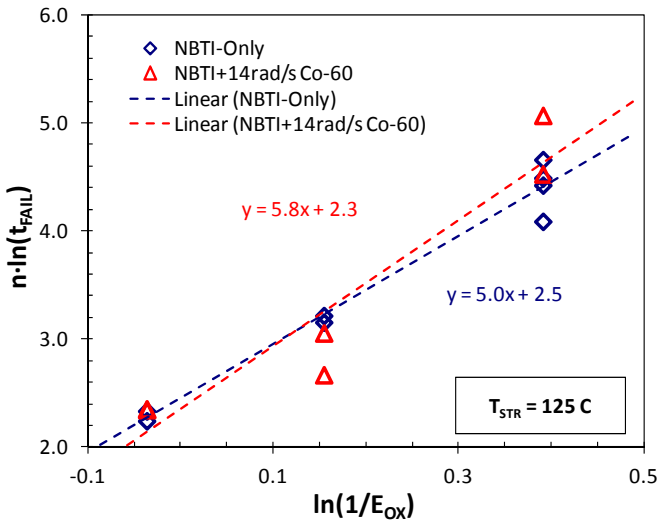

Figure 66. Determining m for ΔV_T as a function of V_{STR} (E_{OX}).

Like E_A, m too is dependent on the extracted value of n and the extrapolated TTF as demonstrated in the equation for m given by

$$m = n \cdot \ln\left(\frac{t_{CRIT(1)}}{t_{CRIT(2)}}\right) \cdot \ln\left(\frac{E_{OX1}}{E_{OX2}}\right). \tag{5.2}$$

The non-linear nature of the NBTI+γ data suggests a potential dependence of ΔV_T on V_{STR} not seen in NBTI-Only data.

d. Summary

In summary, changes in the NBTI parameters were observed. The differences between the NBTI-only versus NBTI+γ were not significant enough to make conclusive assessments regarding the observed changes to n, E_A and m resulting from ionizing radiation. However, ionizing radiation may have introduced a change in m for the dependence of ΔV_T on V_{STR}. In the next section, a trend develops that demonstrates the overall dependence of ΔV_T on V_{STR} versus NBTI-only and NBTI+γ.

3. Experimental Results and Analysis for ΔV_T versus ΔI_{ON}

Preceded by a discussion on the relevance of the I_{ON} parameter to circuit design and NBTI analysis, the presentation and analysis of the fractional ΔV_T versus ΔI_{ON} results

follows revealing somewhat surprising results in the ΔV_T versus ΔI_{ON} relationship as a result of ionizing radiation.

a. Importance of I_{ON}

As previously discussed, NBTI has an unfavorable effect on the V_T, I_{DS}, μ_p, and g_m parameters of the p-channel MOSFET. The I_{ON} parameter, defined as the transistor drive strength for the condition in which I_{DS} is evaluated at $V_{GS} = V_{DS} = V_{DD}$, is a significant parameter to design engineers as it is a measure of the ability of the transistor to drive a load. A degradation in I_{ON} results in a slower transistor which can have an effect on circuit speed and performance. In terms of observing NBTI degradation, the I_{ON} parameter is useful as it can be expressed in terms of the V_T and μ_p parameters that can be directly affected by NBTI [9].

b. Presentation of the Data

In this section, a clearer picture emerges toward determining what effect, if any, ionizing radiation has on the NBTI. Figure 67 presents the per cent change in ΔV_T versus ΔI_{ON} for both the NBTI-only and the NBTI+γ experiments interpolated to a stress time of 80×10^3 seconds.

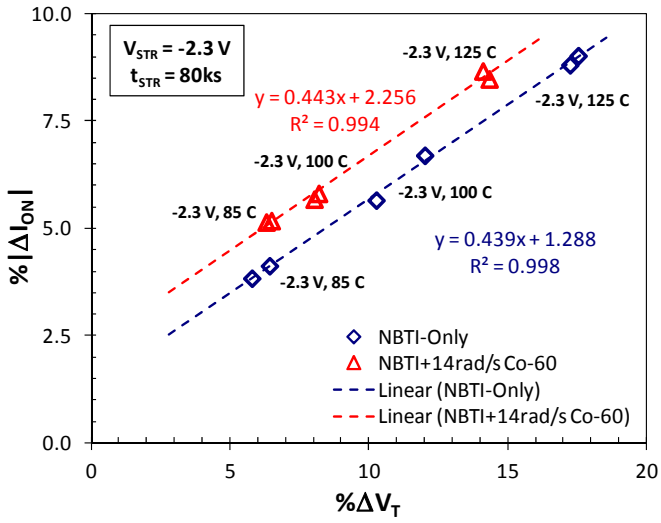

Figure 67. Plot of $\%\Delta V_T$ versus $\%|\Delta I_{ON}|$, NBTI-only versus NBTI+γ, constant V_{STR}.

As illustrated by the best-fit lines, a strong linear dependence was demonstrated between the $\%\Delta V_T$ versus $\%\Delta I_{ON}$ data. Furthermore, as a result of the ionizing radiation, the linear-fit line associated with the NBTI+γ data demonstrated a translation yet remained nearly parallel to the NBTI-only linear-fit line.

The plot of Figure 68 illustrates the effects of ionizing radiation on the relationship between $\%\Delta V_T$ and $\%\Delta I_{ON}$ for the case where V_{STR} was varied.

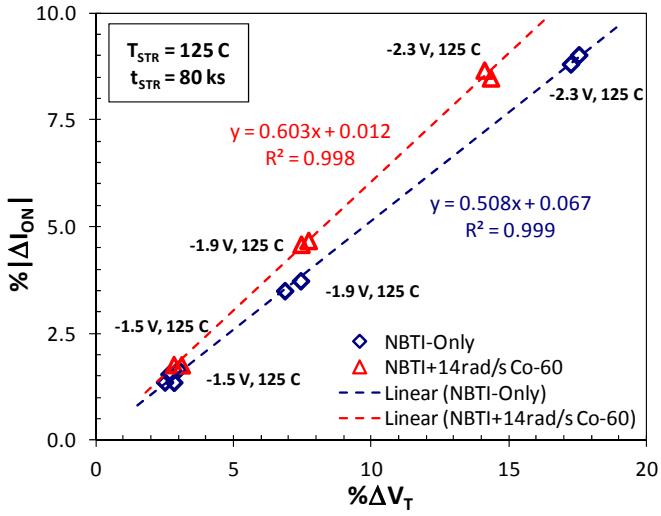

Figure 68. Plot of $\%\Delta V_T$ versus $\%|\Delta I_{ON}|$, NBTI-only versus NBTI+γ, constant T_{STR}.

The best-fit lines to the experimental data demonstrated a slight increase in slope due to the irradiation suggesting field dependence of the irradiation effects on the NBTI responses. Furthermore, like the data of Figure 67, a translation was observed. The NBTI+γ data of Figure 68 suggest that for the high-V_{STR} data point irradiation in the presence of the high electric field had the effect of suppressing ΔV_T by approximately 4% (on a scale of 20%) compared to the NBTI-only counterpart. The two lower V_{STR} points saw both a slight increase in $\%\Delta V_T$ and $\%\Delta I_{ON}$. In other words, irradiation at lower electric fields increased the $\%\Delta V_T$; whereas, irradiation under high-fields suppressed the $\%\Delta V_T$.

Recalling the discussion regarding the relationship between ΔI_{ON} and ΔV_T given in Chapter IV, we established (assuming that the change in ΔI_{ON} was primarily attributed to ΔV_T and the contribution due to $\Delta \mu_p$ was negligible) that

$$\left|\frac{\Delta I_{ON}}{I_{ON-0}}\right| = \frac{\beta}{\left(\frac{V_{DD}}{V_{T0}} - 1\right)} \cdot \frac{\Delta V_T}{V_{T-0}}. \tag{5.3}$$

However, if the contribution of $\Delta \mu_p$ to ΔI_{ON} is not negligible as a result of ionizing radiation or other degradation mechanism, then Equation (5.3) can be adapted to include the term associated with $\Delta \mu_p$ resulting in

$$\left|\frac{\Delta I_{ON}}{I_{ON-0}}\right| = \frac{\beta}{\left(\frac{V_{DD}}{V_{T0}} - 1\right)} \cdot \frac{\Delta V_T}{V_{T0}} + \left|\frac{\Delta \mu_p}{\mu_{p-0}}\right|, \tag{5.4}$$

where the μ_{p-0} term is the pre-stress effective channel mobility. It is well known that the change in the μ_p due to interface traps can be approximated by

$$\Delta \mu_p \approx \frac{\mu_0}{1 + \Delta N_{IT}}, \tag{5.5}$$

where the low-field mobility is given by μ_0. In addition to μ_p being sensitive to changes in the V_T [8] degradation in μ_p can be directly attributed to an increase in radiation induced interface traps N_{IT} [36], [39].

c. ΔI_{ON} versus ΔV_T Dispersion Analysis

The experimental results of the NBTI+γ devices, as compared to the NBTI-only, exhibited a decrease in ΔV_T at V_{STR} = –2.3 V and T_{STR} greater than 85 C; while ΔI_{ON} remained relatively unchanged from their NBTI-only counterparts. This observed dispersion in the data was an unexpected and surprising result of the addition of the ionizing radiation. However, based on Equations (5.4) through (5.5), and recalling that,

$$\Delta V_T = \Delta V_{T-OT} + \Delta V_{T-IT}, \tag{5.6}$$

one could envision the scenario, as supported by the experimental data, where interface trap generation remained unchanged, or increased, while oxide hole trapping decreased as a result of ionizing radiation; in turn, resulting in the observed dispersion. The physical mechanisms suspect in the radiation induced dispersion follows.

d. Possible Physical Mechanisms behind $\%\Delta I_{ON}$ versus $\%\Delta V_T$

With little or no modification to the switched trap models presented by Lelis for radiation and Goes for NBTI the observations of the NBTI+γ experimental data can be explained. Figure 69 illustrate the four switched trap configurations of the E′-center with P_b-center of the switched trap model.

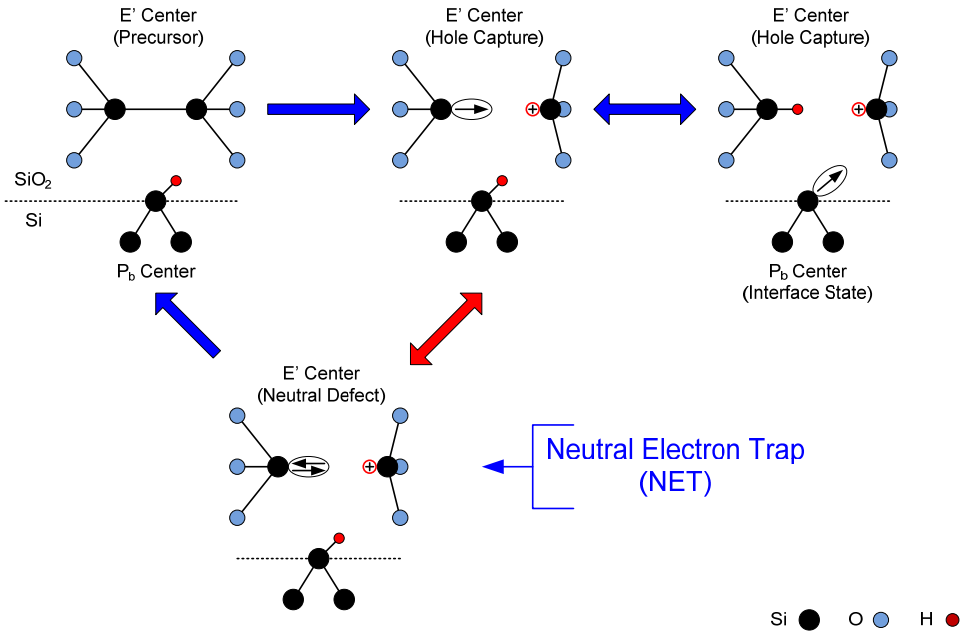

Figure 69. The E′-center precursor, hole capture, hole capture with interface state, and neutral electron trap, after [28], [30].

The E′-center precursor can be activated by ionizing radiation or NBTI. In the activated state the E′-center can exist as either a positively charged hole trap center or a neutral electron trap (NET) center. It is assumed that whether created by ionizing radiation or NBTI, under the two-step process where hole trapping precedes interface state creation in a tightly coupled process, both assist in the facilitation of interface states.

However, based on the experimental data, it could be argued that the radiation induced E′-center can act as a NET under high field conditions.

Whether the NET is a stable configuration or one prone to full recovery into the precursor state or transition back to the hole capture state depends on the location of the E′-center complex. If it is near the interface, once the center undergoes structural relaxation, hole capture and subsequent electron capture, the localized stress at the Si-SiO_2 interface can result in greater separation of the Si-Si atoms, which in turn create a more stable defect. However, if the NET is in a region of relatively lower stress, then the electrostatic force between the two Si atoms tends to reform the Si-Si bond and full recovery can take place [28].

If in fact the NET is acting as a stable neutral E′-center due to irradiation, then the tunneling electron that forms the NET can be viewed as neutralizing a fixed charge near the interface. There is basis for this proposition. Mayberry et al. performed NBTI experiments on PMOS devices with nitrided SiO_2 dielectrics and identified three contributing charge terms. In addition to the charge due to interface states and the recoverable hole-trapping components, they identified a pseudo-permanent component "whose origin remains to be identified" that could be removed (neutralized) by applying a positive bias across the oxide after stressing [40]. This would have the effect of reducing the ΔV_T due to oxide traps while not affecting the interface states; thereby demonstrating the potential for a decrease in ΔV_T while ΔI_{ON} can remain constant due to mobility degradation as a result of N_{IT}.

Where Mayberry achieved the neutralization by applying a positive bias to the gate with respect to the source/drain/bulk terminals, the work performed in this dissertation neutralized the irradiation induced positive oxide-charge defect by electron tunneling from the gate terminal through the oxide at high V_{STR} (E_{OX}). In work performed by Nishida and Thompson [41], "as-fabricated traps" in SiO_2 oxides could be filled with a substrate-injection of electrons. A key element of their research was that the ΔV_T (or $\Delta V_{G\text{-}OT}$) was that the amount of electron trapping was dependent on the injection fluence and the electric field across the oxide as demonstrated in the data presented in Figure 70.

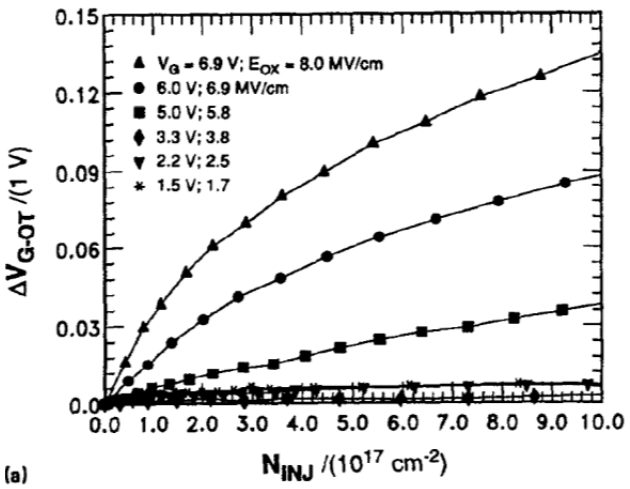

Figure 70. Gate voltage shift vs. injected electron fluence for 8.6 nm oxide, from [41].

As demonstrated in the data presented in Figure 71, for a fixed electron fluence of $6 \times 10^{17}/\text{cm}^2$ the dependence of the trapped oxide charge is given as a function of electric field.

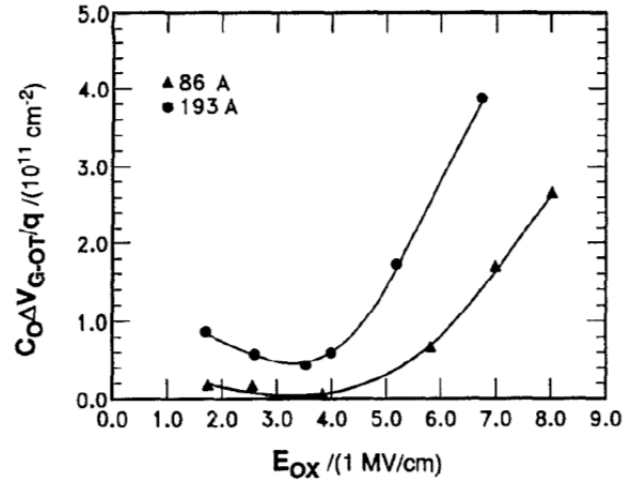

Figure 71. Steady-state $\Delta V_{G\text{-}OT}$ vs. E_{OX} for an electron fluence of $6 \times 10^{17}/\text{cm}^2$, from [41].

For the devices researched under this dissertation, the electron fluence given by Nishida and Thompson would equate to about 5 nA of gate current. Given the elevated temperature and high electric field (100 C and 7 MV/cm) seen by these devices at the higher stress conditions a tunneling current of 5 nA is reasonable. The reduction of ΔV_T

by ~4% (10 mV) demonstrated in Figure 70 comparing NBTI-only to NBTI+γ equates to the a reduction in the total number of oxide traps on the order of ~1×10^3 or a neutralized trap density of $N_{OT} \sim 1 \times 10^9/\text{cm}^2$.

The significance of these findings is that as a result of ionizing radiation oxide traps can be neutralized while the interface state generation is not affected correspondingly and hence the change of slope and offset in the $\%\Delta I_{ON}$ versus $\%\Delta V_T$ curves given previously in Figures 67 and 68.

However, more compelling evidence for electron trapping came from work performed by Busani, Devine, and Hughes in which it was demonstrated that Fowler-Nordheim (FN) tunneling during NBTI characterization at high V_{STR} had the effect of reducing ΔV_T by trapping electrons in the oxide while not reducing the channel mobility degradation [42]. In their work, PMOS transistors with nitrided SiO_2 dielectrics were subjected to NBTI stresses of room temperature T_{STR} and –2.4 V V_{STR}. The T_{STR} was chosen to minimize the NBTI effect which allowed for the characterization of the $-\Delta V_T$ due to trapped electrons in the oxide as a result of FN tunneling. They then performed the same NBTI experiment but with T_{STR} set to 150 C. The data from both experiments are presented in the plots of Figure 72.

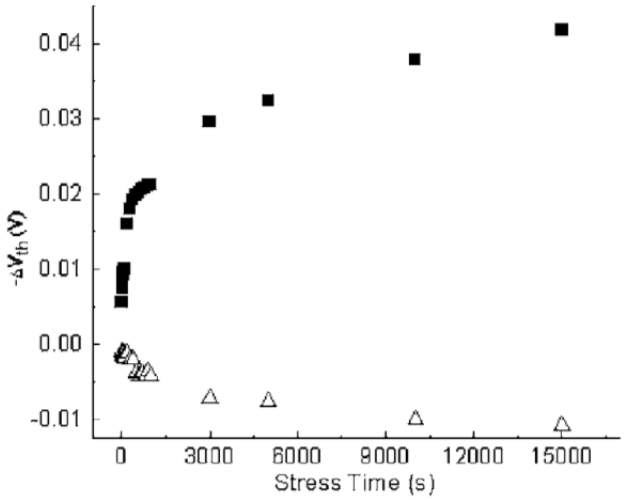

Figure 72. ΔV_T induced by NBTI at 150 C (■) and by FN electron tunneling at room temperature (Δ), from [42].

They concluded that, at high V_{STR} and T_{STR} of 150 C, electron trapping in the oxide due to FN tunneling was compensating for the ΔV_T due to NBTI.

The significance of their research resides in the fact that the NBTI induced ΔV_T TTF calculations from devices stressed in the FN regime will underestimate the ΔV_T extrapolated to a lower operating V_{STR}. This underestimation of ΔV_T has the effect of overestimating the device lifetime. Busani et al. realized this and estimated that, for the devices in their study, lifetimes could be overestimated by a factor of two. The data presented in Figure 73 illustrates the ΔV_T from the combined mechanisms of NBTI and FN tunneling versus ΔV_T from NBTI with the FN component removed.

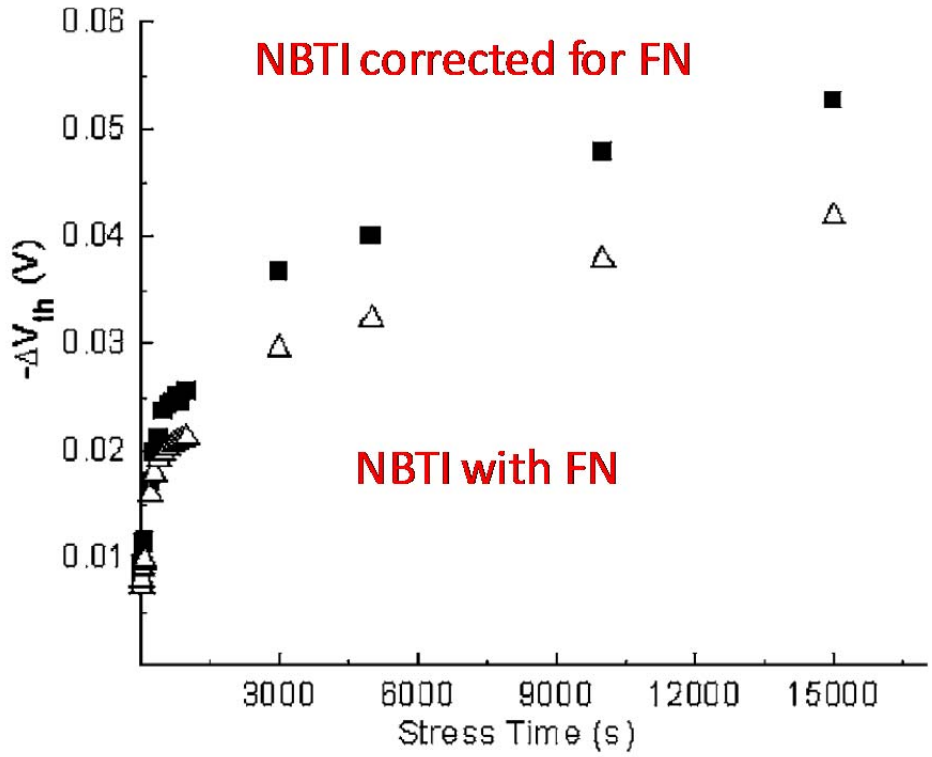

Figure 73. NBTI ΔV_T with FN (Δ) and with FN component removed (■), after [42].

With respect to the research performed in this dissertation, their findings suggests that by irradiating the devices the threshold needed for FN tunneling (which is a function of electric field across the oxide provided by V_{STR}) can be lowered. This lowering is due

to the ionizing radiation creating trap centers in the oxide near the gate-poly conduction band, which, in turn, leads to trap assisted FN tunneling of electrons into the oxide and a subsequent neutralization of NBTI induced hole traps. It is this neutralization process, as demonstrated in the band diagrams of Figure 74, that reduces ΔV_T.

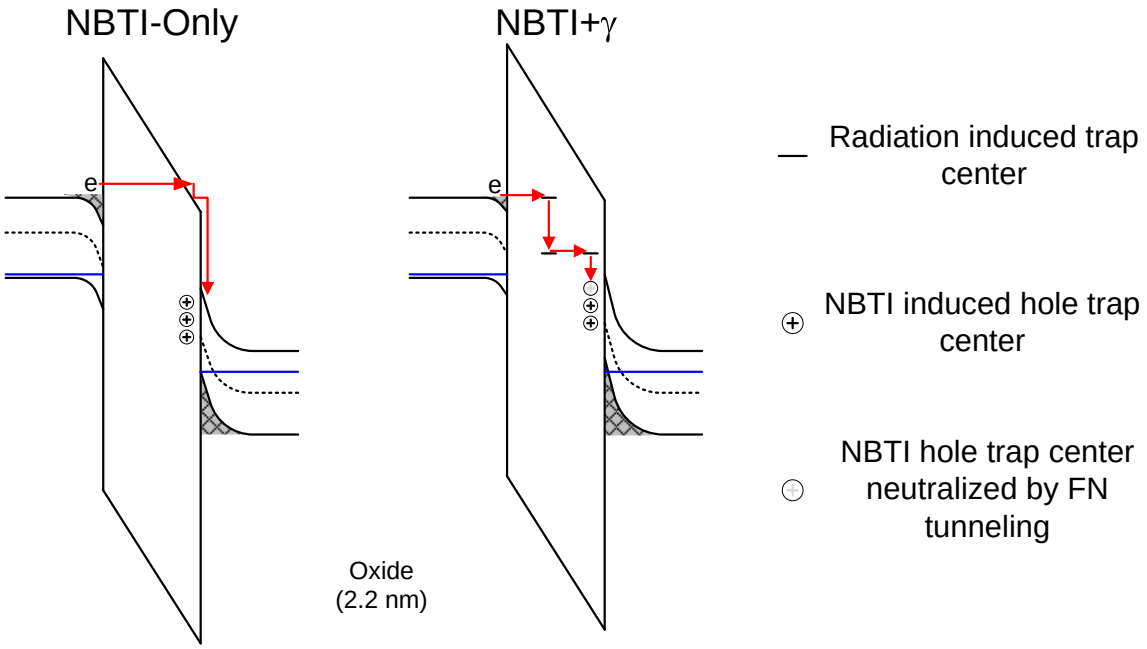

Figure 74. FN tunneling; without radiation (left), radiation trap assisted (right).

Without ionizing radiation (the NBTI-Only case), for FN tunneling to occur, the entire width of the barrier presented by the oxide must be overcome. Those electrons that do overcome the barrier end up in the Si conduction band. However, with the trap centers provided by the ionizing radiation (the NBTI+γ case) the tunneling distance is reduced thereby allowing electrons to tunnel into the oxide where they can neutralize hole traps.

The experimental data given in Figure 75 demonstrates the reduction in ΔV_T consistent with Busani with the suspected physical mechanism being radiation induced trap centers allowing FN tunneling of electrons to occur, which subsequently neutralize NBTI induced hole traps.

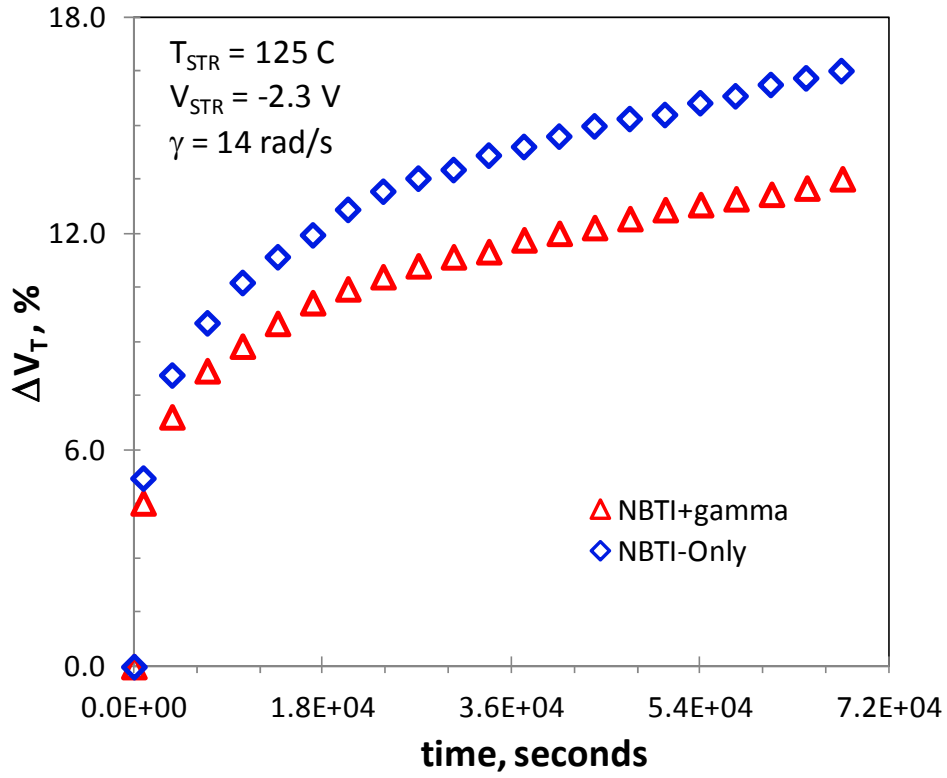

Figure 75. The plot of $\%\Delta V_T$ vs. time comparing NBTI-Only and NBTI+γ.

4. Radiation Dependence of the ΔI_{ON} to ΔV_T Ratio

It was desired to determine what effect ionizing radiation had on the NBTI response to dose rate, total dose, and post-TID anneal conditions. Since the $\%\Delta I_{ON}$ relationship with $\%\Delta V_T$ emerged as an indicator to observe the changes to the NBTI response as a result of ionizing radiation, it became apparent than an examination of the ratio of the $\%\Delta I_{ON}$ to $\%\Delta V_T$ would be instructive.

Toward that end, a summary of the experiments conducted at 125 C are presented in Figure 76 comparing the results from NBTI-only, post-TID and anneal NBTI, and NBTI+γ experiments.

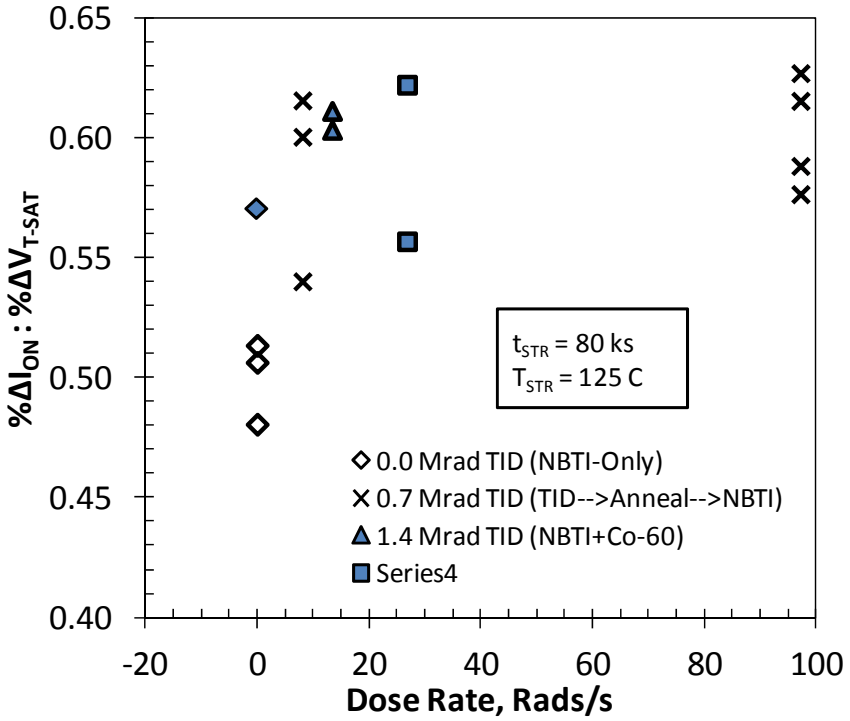

Figure 76. Ratio of $\%\Delta I_{ON}$ to $\%\Delta V_T$ versus dose rate.

In examining the post-TID NBTI (TID→Anneal→NBTI) results no apparent dependence on dose rate or anneal condition were observed. However, an increase in the ΔI_{ON}-ΔV_T ratio was observed. The NBTI+γ devices also exhibited an increase in the ratio and that ratio seemed to be dose dependent, though that dependence is suspect due to the limited number of experimental samples. The filled data symbols represent experiments performed with the Dewar temperature system (DTS) used with the J. L. Shepherd irradiator; whereas, the NBTI-only and post-TID NBTI experiments used the Tenney oven for temperature control.

Since the devices did not demonstrate sensitivity to dose rate or anneal, the plot of Figure 77 represents the same data as a function of TID; and, in Figure 78 the ratios were averaged at each TID to expose potential total dose related trends in the data.

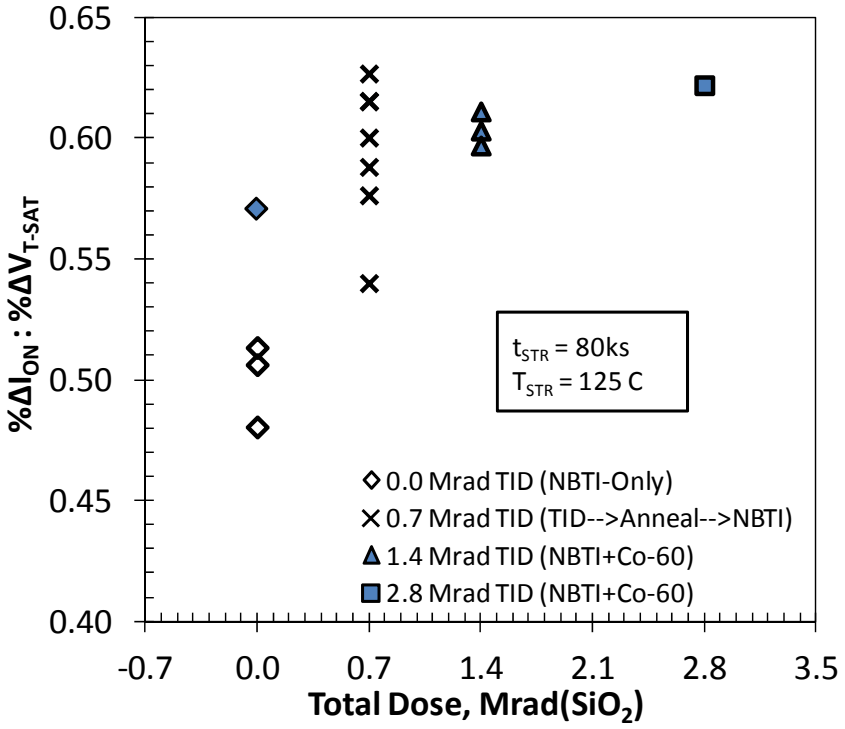

Figure 77. Ratio of $\%\Delta I_{ON}$ to $\%\Delta V_T$ versus total dose.

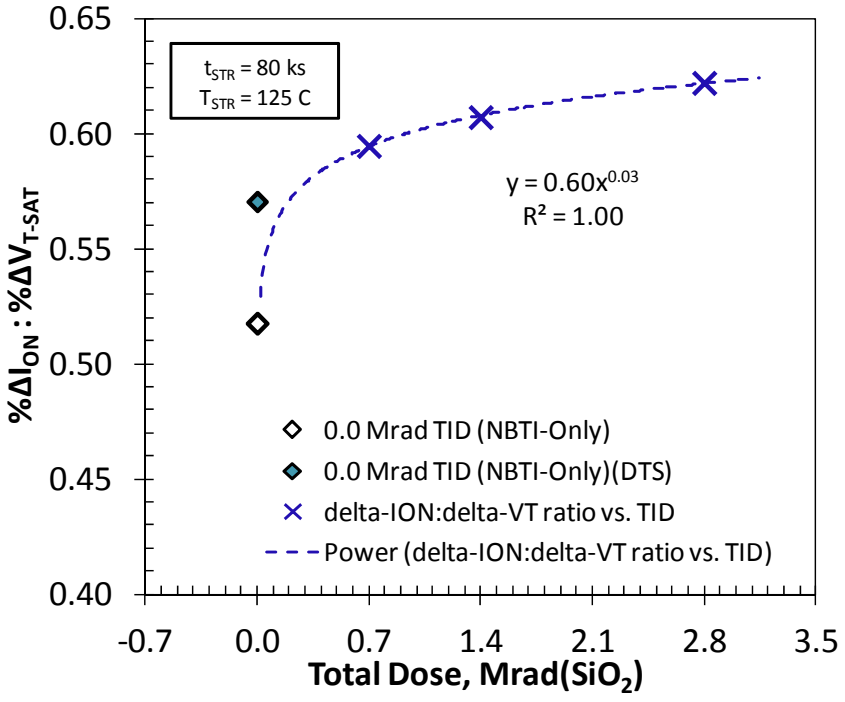

Figure 78. Averaged $\%\Delta I_{ON}$ to $\%\Delta V_T$ ratio versus TID.

A potential outlier, the data point for the NBTI-Only at 0-TID using the DTS remains in the plot for context. Otherwise, the best-fit line exhibits a power-law dependence extrapolated back to the NBTI-only average at 125 C. Because the experimental data used in the plot includes a mixture of stress voltages and experimental methods, the purpose of the plot was to reveal a potential relationship between TID and the ΔI_{ON}-ΔV_T ratio.

5. Summary

The results of NBTI-only versus NBTI+γ experiments were presented highlighting new and unexpected observations surrounding the effects of ionizing radiation on NBTI. These surprising results demonstrated that radiation had an effect on NBTI which was characterized by an increase in the NBTI at for values of V_{STR} approaching operationally relevant conditions and was reduced at high V_{STR}.

This reduction was observed for devices receiving radiation prior to and during NBTI. This reduction in NBTI is considered to be due to the irradiation assisted neutralization of oxide traps at the near-interface E′-centers. However, since the $\%\Delta I_{ON}$ appeared to be held nearly constant while $\%\Delta V_T$ decreased, along with the observed slope change and offset in the $\%\Delta I_{ON}$ vs. $\%\Delta V_T$ linear fit line of the NBTI+γ devices gives evidence that the apparent decrease in μ_p was a result of an increase in N_{IT} production while the hole trap process mediating the N_{OT} production can be subsequently neutralized in the presence of a tunneling current at high field conditions due to FN tunneling.

The key finding of this research is that, for the first time, the effects of ionizing radiation on the NBTI of PMOS devices demonstrated that $\Delta\mu_p$ played a significant role and presents a viable explanation for the observed data consistent with the carrier transport theories offered in support.

C. COMBINED EFFECTS MODEL

The $\%\Delta I_{ON}$ versus $\%\Delta V_T$ data presented in the previous section confirmed what was observed in the analysis of $\%\Delta V_T$ alone. The parallel translation of the best-fit lines (without change of slope) in going from the NBTI-only to the NBTI+γ case supports the

observation that the activation energy for ΔV_T was not affected by the irradiation. For the case of constant T_{STR}, the slope change with translation of the linear best-fit lines supports the observation that the dependence of ΔV_T on V_{STR} had changed due to the irradiation. The addition of the $\%\Delta\mu_p$ term in Equation (5.5), to a first-order, accounts for changes in the relationship between $\%\Delta I_{ON}$ and $\%\Delta V_T$ due to changes in μ_p.

At the onset of this research, a revised version of the generally agreed on model for ΔV_T due to the combined effects of NBTI and irradiation was expected. However, in light of the unique and surprising results of this research and data, a revised model which includes the $\Delta\mu_p$ term that accounts for the radiation and its effects is needed. Therefore, a new model is proposed that in its simplest form accounts for the effects of the radiation where ΔI_{ON} is now a function of ΔV_T and $\Delta\mu_p$. For the old model representing the NBTI-only case, the $\%\Delta I_{ON}$ was given by

$$\left|\frac{\Delta I_{ON}}{I_{ON-0}}\right| = \frac{\beta}{\left(\frac{V_{DD}}{V_{T0}} - 1\right)} \cdot \frac{\Delta V_T}{V_{T0}} + \left|\frac{\Delta \mu_p}{\mu_{p-0}}\right|, \tag{5.7}$$

in which the $\Delta\mu_p$ term was negligible and therefore resulted in

$$\Delta I_{ON} = \Delta V_T \left(V_{STR}, T_{STR}\right). \tag{5.8}$$

In contrast to the result of Equation (5.8) for the NBTI+γ case, the new model representing $\%\Delta I_{ON}$ as a function of ionizing radiation is given by

$$\Delta I_{ON} = \Delta V_T \left(V_{STR}, T_{STR}, Dose\right) + \Delta \mu_p \left(V_{STR}, Dose\right). \tag{5.9}$$

In the constant V_{STR} case for ΔV_T versus ΔI_{ON}, $\Delta\mu_p$ is now a function of ionizing dose; whereas, for the constant T_{STR}, $\Delta\mu_p$ is a function of both V_{STR} and ionizing dose. The details of this model are the subject of future work to follow.

D. CONCLUSION

In this chapter, data on the combined effects of NBTI and ionizing radiation on the p-channel MOSFET was presented. It was demonstrated that no significant changes were observed in the parameters used to characterize ΔV_T. Yet, ionizing radiation had an

influence on the NBTI response characterized by a slight but perceptible increase in the NBTI approaching operationally relevant V_{STR} and significant decrease in the NBTI at high V_{STR}. Furthermore, the changes observed in the relationship between $\%\Delta I_{ON}$ and $\%\Delta V_T$ suggests that characterizing ΔV_T is not useful in fully characterizing the changes in transistor performance due to NBTI and ionizing radiation.

Though the NBTI extracted parameters varied slightly from the process model. The relationship between the $\%\Delta I_{ON}$ and $\%\Delta V_T$ was highly correlated in both the NBTI-only and NBTI+γ experiments. From this tight dependence of $\%\Delta I_{ON}$ on $\%\Delta V_T$, the impact of the ionizing radiation on PMOS NBTI became observable.

Another finding from the data was observed dispersion in the $\%\Delta I_{ON}$ versus $\%\Delta V_T$ data. One possible explanation for the dispersion in the decreased ΔV_T at higher V_{STR} in the presence of radiation was the activation of E′-centers that could then trap electron injected into the oxide by radiation assisted FN tunneling in turn lowering the contribution of $\Delta V_{T\text{-}HT}$ to the overall ΔV_T.

A significant outcome related to the observed dispersion is that the use of a high V_{STR} to accelerate NBTI, in the presence of radiation, will lead to an underestimate of the combined effects on ΔV_T if extrapolated to an operationally relevant V_{STR} condition.

Finally, a new combined effects model for ΔI_{ON} was offered that accounts for the effects of the radiation on ΔI_{ON} as a function of both ΔV_T and $\Delta \mu_p$. This model, which is the subject of future work, can be developed to gain additional insight into the effects of ionizing radiation on PMOS NBTI.

VI. CONCLUSIONS

PMOS NBTI in an Ionizing Radiation Environment set out to determine what effect, if any, ionizing radiation has on the most pressing reliability concern in modern semiconductor devices, PMOS NBTI. Though lots of early work had been done on radiation effects under various stress bias and temperature conditions, most of that research was performed on NMOS devices as they were seen as more susceptible to a loss of electrostatic control and unacceptable levels of leakage current as compared to their PMOS counterpart. Furthermore, with decreasing oxide thickness it was believed that, with the exception of NMOS devices in buried oxides, modern devices were becoming radiation hardened. This belief had with it forty-plus years of experience dealing with the same, well characterized, material system: SiO_2 dielectrics and Si-SiO_2 interfaces.

However, with the introduction of new material systems, namely high-k dielectrics, there is uncertainty in how these devices will perform in a radiation environment. This same device scaling and introduction of new material systems brought with it a re-emergent and significant reliability concern of NBTI in PMOS devices for which the physical mechanisms responsible are not fully understood and hotly debated.

None the less, the semiconductor industry as a whole has been more focused on the consumer electronics market in which products need only last a few years as opposed to the ten or twenty a military or aerospace application may depend on in an ionizing radiation environment; hence the motivation for this work.

In the discussion that follows, a summary of the research performed, its findings, significant contributions, and opportunities for future work is presented.

A. SUMMARY OF RESEARCH PERFORMED AND FINDINGS

Commercially available p-channel MOSFETs from a 130 nm CMOS technology were put through a series of experiments to ascertain their susceptibility to a combination of ionizing gamma-ray radiation and NBTI. Chapter II gave background on the theory of the MOSFET V_T and addressed PMOS NBTI and radiation effects. Included in the

discussion on NBTI were the two competing theories that offer physical explanations for the observed effects, the long-standing hydrogen reaction-diffusion model and the emergent switched-trap model. Chapter II concluded with the notion that the combined effects of NBTI and radiation could possibly be worse than the sum of the effects taken separately.

In Chapter III, the experimental approach and platform for evaluating the combined effects was laid out. This approach, or methodology, outlined the performance of NBTI characterization in the spirit of the JEDEC standard for NBTI testing (JESD90) and the MIL-STD-883 standard for radiation effects testing (Method 1019.8). Two types of experiments were devised, one for performing NBTI characterization after irradiation and anneal, the other with the objective of performing NBTI characterization while the devices were being irradiated. Due to a limited knowledge of the material system under study, a series of experimental conditions were identified to look for irradiation, bias, and anneal sensitivities. The platform developed specifically for carrying out the experiments included the Keithley 4200-SCS which allowed for the stress and measure of four devices simultaneously, the DMEA SEGIT J. L. Shepherd irradiator with the Dewar temperature system, and the Tenney environmental oven.

The experimental results and analysis of the NBTI-only experiments were presented in Chapter IV; but not before an examination of the manufacturer's process model was performed. This examination included the decomposition of the model for the purpose of isolating the main NBTI dependent parameters. These consisted of the time-exponent n, the activation energy E_A, and the electric field exponent, m. Numerical and graphical methods were established for extracting these parameters from the experimental data. This was followed by the presentation and analysis of the NBTI-only experiments given in the context of the process model. A quantitative analysis then followed that demonstrated the relationship between the fractional changes in I_{ON} versus V_T. This relationship was supported by the experimental data and established a framework for evaluating devices subjected to the combined effects of ionizing radiation and NBTI.

The combined effects results and analysis were given in Chapter V. It was demonstrated that ionizing radiation had an influence on the NBTI response characterized

by an increase in the NBTI approaching operationally relevant V_{STR} and significant decrease in the NBTI at high V_{STR}. A significant outcome of this work is that the use of a high V_{STR} to accelerate NBTI, in the presence of radiation activated trap centers, will lead to an underestimate of the combined effects if extrapolated to an operationally relevant V_{STR} condition. Though the NBTI extracted parameters could not be distinguished from the process model, the relationship between the $\%\Delta I_{ON}$ and $\%\Delta V_T$ was highly correlated in both the NBTI-only and NBTI+γ experiments. From this tight dependence, the impact of the ionizing radiation on PMOS NBTI became observable; and, from an examination between the ratios of ΔI_{ON} to ΔV_T versus TID a dependence on ionizing dose emerged. Finally, a combined effects model was introduced representative of the combined effects of ionizing radiation and NBTI on ΔI_{ON} as a function of ΔV_T and $\Delta \mu_p$.

B. SIGNIFICANT CONTRIBUTIONS AND PUBLICATIONS

1. Significant Contributions

There are a number of significant contributions that add to the body of scientific knowledge as a result of this research. These contributions include:

- The demonstration that ionizing radiation has an effect on PMOS NBTI
- The use of NBTI characterization methods for evaluating the effects of ionizing radiation on PMOS NBTI
- Development of a model for ΔI_{ON} that includes the effects of ionizing radiation on NBTI
- The development of the test and measurement system required to perform the experiments needed for the all of the above contributions

The first bullet is of interest to the reliability physics community and may spur follow-on research within that community toward resolving the hotly debated physical mechanisms responsible for NBTI. Furthermore, the knowledge that ionizing radiation may exacerbate PMOS NBTI is of immediate interest to the military and aerospace systems design communities.

The second bullet is also of interest to the reliability physics community as it provides a method for examining the combined effects of NBTI and ionizing radiation on PMOS NBTI. Moreover, combining the NBTI characterization standard and ionizing

radiation gives reliability engineers tasked with evaluating and characterizing technologies targeting military and aerospace applications a method for evaluating the combined effects.

The third bullet is of interest to the reliability physics, engineering, and design communities. Though the mathematical model is preliminary it identifies a mathematical relationship between ionizing radiation and NBTI that can be developed further and applied to new and emerging material systems and technologies of interest to the military and aerospace communities.

The ability to do combined effects analysis under operationally relevant conditions has been gaining interest of late; therefore, the final bullet is of interest to those wanting to perform combined effects analysis for the purpose of device, circuit, and system development, evaluation, and validation.

2. Publications

Technical publications resulting from this research include two poster manuscripts titled "PMOS NBTI analysis of a 45 nm CMOS-SOI Process with Nitrided Gate Dielectric" and "On the Device Response of a 45 nm PMOS Transistor to TID and NBTI Stresses" published in the proceedings of the 2012 IEEE International Integrated Reliability Workshop (IIRW) and the 2013 Government Microcircuit Application & Critical Technology (GOMACTech) conference respectively.

In addition, at least two journal manuscripts based on the aforementioned significant contributions are currently planned for submission to publications of the IEEE. These publications include the Transactions on Device and Material Reliability (The use of the NBTI Characterization Framework for Evaluating the Effects of Ionizing Radiation on NBTI), the Electron Device Letters (The Dependence of PMOS NBTI on Ionizing Radiation—Early Results), and the Transactions on Nuclear Science (The Effect of Ionizing Radiation on NBTI). Finally, the work has started for the Patent Application process for the unique combined effects test and measurement system.

C. OPPORTUNITIES FOR FUTURE WORK

All of the significant contributions listed in the previous section had an implied prospective opportunity for extended research in the area of combined effects analysis. In addition to those listed, the following are viable in extending the work of this dissertation,

- A further development of the proposed combined effects model
- An extension of this research to identify physical mechanisms responsible for the combined effects observations
- An extension of this work to technologies relevant to the military and aerospace communities.

In order to further develop the proposed combined effects model, a deeper understanding of the combined effects or radiation and NBTI on μ_p is needed. Toward that goal, future research on the existing data produced from this work can be used to evaluate changes in the subthreshold slope (an indicator of $\Delta\mu_p$).

An extension of this work to include the analysis of the contributions of interface trap generation and hole trapping to the changes observed in the combined effects experiments can be accomplished by taking a formal look at the radiation effects. The work performed in this dissertation looked primarily at 1.4 Mrad TID (14 rad/s). Extending this work to a range of total doses and dose rates would serve to help identify the physical mechanisms responsible for the combined effects interaction and could lead to a better understanding of the physical mechanisms responsible for changes in ΔI_{ON}, ΔV_T, and $\Delta\mu_p$.

Furthermore, the observations of FN tunneling in devices subjected to irradiation needs to be explored further. Research is needed to characterize the sensitivities of FN tunneling and the associated oxide and interface trap dynamics to total-dose, dose-rate, V_{STR} and T_{STR} effects. As was demonstrated in this work, this unexpected physical mechanism has the potential for altering TTF calculations at the detriment of DoD fielded systems. A greater understanding of what is happening at the physical level would go a long way toward mitigating risk in TTF and reliability analysis.

Finally, an extension of this work within the 130 nm technology and other technology nodes of interest would greatly benefit the military and aerospace communities. For example, a study of the thick-oxide devices within the 130 nm technology would help in the understanding of how oxide thickness plays a role in the oxide and interface trap kinetics that could be extended to other technologies of interest to the DoD.

APPENDIX A. TEMPERATURE CORRECTION OF V_T

A. DATA CORRECTION OF ΔV_T DUE TO ΔT

If temperature fluctuations during an experiment are significant enough to introduce considerable errors in the measurements, then data recorded during the experiment are required to be corrected. For the V_T, it has a significant dependence on temperature; therefore, a method to normalize the data was developed.

The V_T temperature dependence of the PMOS devices in this process was characterized. It was shown that, as in Figure 79, the V_T *vs.* T relationship was linear and consistently produced a $\Delta V_T/\Delta T$ temperature coefficient of 0.72 mV/C.

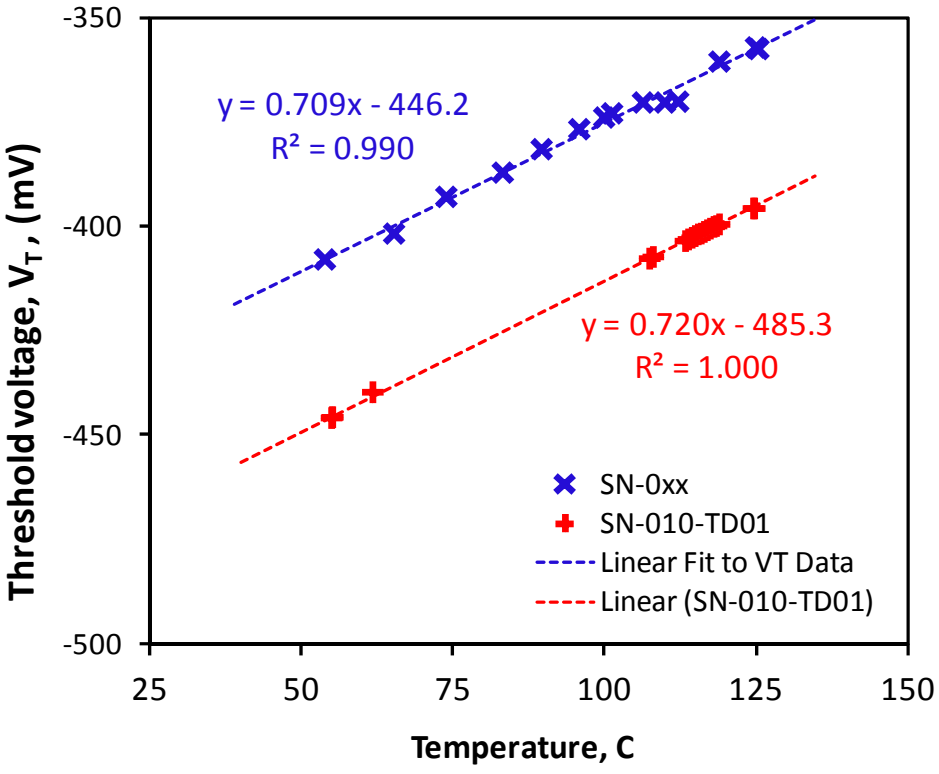

Figure 79. Demonstrated threshold voltage dependence on temperature.

Given the characteristic slope $m = \Delta V_T/\Delta T$ and knowledge of the temperature variation as a function of experiment time, data recorded during the experiments could be corrected by

$$V_{T-Corr} = V_{T-Meas} + m\ (T_{\mu} - T_{Meas}). \tag{7.1}$$

The mean temperature T_{μ} is time average of the temperature recorded during the experimental period during which data was collected. The data shown in Figure 80 demonstrates a significant difference in the linear fit of the data to regression analysis and a notable shift in the amplitude of V_T change.

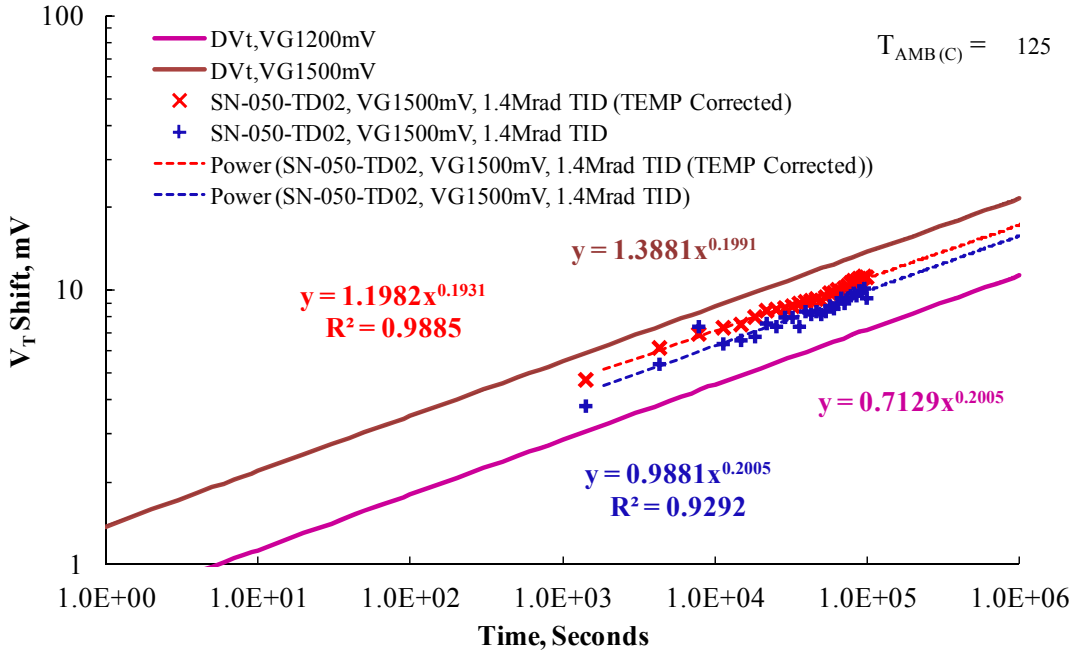

Figure 80. Plot of measured data vs. temperature corrected data.

APPENDIX B. ELECTRICAL CONDITIONS FOR MEASURING V_T

The electrical parameters for measuring V_T are given in Table 10.

Table 10. Table of conditions for measuring V_T for the 130 nm CMOS devices.

PMOS Drain Currents, I_D for $V_T = V_{GS}(I_D)$

I_{VGSi} (uA)		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	23	12
	260	152	76

I_{VGSi} (uA) CEILING = 5		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	25	15
	260	155	80

I_{VGSi} (uA) CEILING = 10		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	30	20
	260	160	80

PMOS Test Devices		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	TD01-03	TD01-03
	260	TD05	TD05

NMOS Drain Currents, I_D for $V_T = V_{GS}(I_D)$

I_{VGSi} (uA)		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	100	50
	260	650	325

I_{VGSi} (uA) CEILING = 5		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	100	50
	260	650	325

I_{VGSi} (uA) CEILING = 10		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	100	50
	260	650	330

NMOS Test Devices		LV: L_{des} (um)	HV: L_{des} (um)
		0.120	0.240
W_{des} (um)	40	TD01-03	TD01-03
	260	TD05	TD05

Conditions for V_T Measurements performed in this research:

$I_{VGSi} = |I_D| = 300$ nA*(W_{des}/L_{des}) for a NMOS device.

$I_{VGSi} = |I_D| = 70$ nA*(W_{des}/L_{des}) for a PMOS device.

PMOS LV Devices:

V_{tlin}, VD = -/+ 50mV; for W/L = 5/5 V_{tlin} = -0.225 +/- 0.045 V

V_{tsat}, VD = -/+ 1200mV; for W/L = 10/0.12 V_{tsat} = -0.300 +/- 0.050

PMOS HV Devices:

Vtlin, VD = -/+ 50mV; for W/L = 5/5 Vtlin = -0.420 +/- 0.060 V

Vtsat, VD = -/+ 2500mV; for W/L = 10/0.12 Vtsat = -0.440 +0.075 -0.095

T = 25°C for comparative purposes to tabled data for V_T

I_{VGSi} (uA) values used in experiments are larger than indicated above (50 and 250uA, respectively)

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